A MATCHED FILTER AND COHERENT DIGITIZER FOR PULSED DOPPLER RADAR SYSTEMS

A Dissertation

by

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ABSTRACT

In this dissertation, a matched filter and coherent digitizer will be presented for pulsed Doppler radar systems. The matched filter is used to filter as much out-of-band thermal noise in the received signal as possible while maintaining pulse shape integrity for various transmitted pulse widths. The coherent digitizer is used to digitize the filtered pulse and recover the Doppler frequency tone, which is often buried in noise and in the presence of large blockers.

A configurable bandwidth filter is presented to be used as a matched filter in a pulsed Doppler radar system. To eliminated dispersion effects in the received waveform, a finite impulse response (FIR) topology is proposed which has a measured standard deviation of in-band group delay of 11.0 ns that is primarily dominated by the inherent delay introduced by the sample-and-hold. The filter is designed to operate at an intermediate frequency (IF) of 40 MHz while being tunable in bandwidth from 3 to 30 MHz, making it optimal for radar systems with varying pulse widths. Employing a total of 128 taps, the FIR filter provides greater than 50 dB sharp attenuation in the stop-band in order to minimize all out-of-band noise in the low SNR received radar signal.

Due to the FIR filter being discrete-time in nature, an anti-alias filter must be used to avoid out-of-band frequency components folding back in-band after sampling. A continuous-time filter based on current-reuse differential difference amplifiers, which is used as an anti-alias filter, will be presented. The two differential pairs in the differential difference amplifier process two independent input signals but share the same output and bias current. To demonstrate the achievable power savings, a 6th order lowpass Butterworth filter was designed, achieving a 65-MHz

-3-dB frequency, an in-band input-referred third-order intercept point of 12.0 dBm, and an input referred noise density of 40 nV/Hz$^{1/2}$, while only consuming 8.07 mW from a 1.8 V supply.

Following the matched filter is a coherent subsampling digitizer. Prior to transmission, the radar system modulates the RF pulse with a known pseudorandom BPSK sequence. Upon reception, the radar digitizer uses a programmable sample-and-hold circuit to multiply the received waveform by a properly time-delayed version of the known BPSK sequence. This operation demodulates the desired echo signal while suppressing the spectrum of all in-band non-correlated interferers, making them appear as noise in the frequency domain. The resulting demodulated narrow-band Doppler waveform is then subsampled at the IF frequency by a $\Delta\Sigma$ modulator. Because the digitization bandwidth within the $\Delta\Sigma$ feedback loop is much less than the input bandwidth to the digitizer, the thermal noise outside of the Doppler bandwidth can be effectively filtered prior to quantization, providing an increase in SNR at the digitizer's output compared to the input SNR.

In this demonstration, a $\Delta\Sigma$ correlation digitizer is fabricated in a 0.18 μm CMOS. The digitizer has a power consumption of 1.12 mW with an IIP3 of 7.5 dBm. The digitizer is able to recover Doppler tones in the presence of blockers up to 40 dBm greater than the Doppler tone.

DEDICATION

To my family

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As I near the end of my graduate school career, I would like to take a moment to look back and thank the many people who have helped me along the way. Without their patience and understanding, I would not have made it to this final stage.

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NOMENCLATURE

$\Delta\Sigma$	Delta Sigma
AC	Alternating Current
ADC	Analog-to-Digital Converter
BAW	Bulk Acoustic Wave
BPSK	Binary Phase Shift Keying
CDP	Conventional Differential Pair
CMFB	Common-Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DC	Direct Current
DDA	Differential Difference Amplifier
DSP	Digital Signal Processor
DUT	Device Under Test
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FoM	Figure of Merit
GBW	Gain-Bandwidth Product
HD_3	Third Order Harmonic Distortion
IF	Intermediate Frequency
IIP3	Third Order Intercept Point
LFM	Linear Frequency Modulated
MUX	Multiplexer

NTF	Noise Transfer Function
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PE	Power Efficiency
PVT	Process, Voltage, and Temperature
RF	Radio Frequency
SAW	Surface Acoustic Wave
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SOI	Silcon-on-Insulator
SQNR	Signal-to-Quantization-Noise Ratio
STF	Signal Transfer Function
VCO	Voltage Controlled Oscillator

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1. INTRODUCTION

In the early years of the 20th century, scientists experimented with detecting electromagnetic waves that have been reflected off of objects beginning a new field of research which would become known as radar. In the 1930s just prior to World War II, much development of radars was done for target detection and range determination. In fact, this is where radar gets its name, *ra*dio *d*etection *a*nd *r*anging [1]. Figure 1.1 shows a basic example of a radar. The radar transmits an electromagnetic wave toward a target. The target reflects the wave back toward the antenna where it will be captured and analyzed by the system.

Modern radars have evolved from systems that just detect targets and determine their range to systems which identify, image, and classify targets as well. They are able to suppress unwanted interference such as echoes from the environment, known as *clutter*, and countermeasures, known as *jamming*.

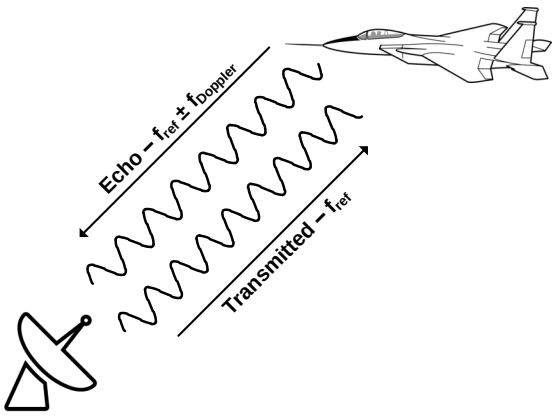


Figure 1.1: A simple radar example.

1.1 Radar Basics

A radar is an electrical system that transmits RF electromagnetic waves toward a region of space and receives and detects those electromagnetic waves when reflected from objects in that region [2]. Radars can be divided into two general classes: continuous-wave and pulsed. In a continuous wave radar two antennas must be used – one for the transmitter and one for the receiver. Since isolation between the two antennas is not perfect, there will always be leakage from the transmitter antenna to the receiver antenna. Because of this, continuous-wave radar is generally limited to lower power designs limiting them to short range applications. In order to determine range to an object, the characteristics of the transmitted waveform cannot be constant; often the frequency of the transmitted waveform is varied with some modulation scheme as linear frequency modulation (LFM – a frequency chirp) which essentially creates a timing mark [2].

In a pulsed radar, the electromagnetic waves are transmitted during a short pulse, generally in the range of 0.1 to 10 μs but can be as short as a few nanoseconds or in the millisecond range. Pulsed radars have two major benefits: 1) only one antenna is needed since the receiver can be used during the transmitter's off-phase, and 2) the receiver can be turned off completely during transmission allowing complete isolation between transmitter and receiver. This allows pulsed radars to operate at much higher power and ranges than their continuous-wave counterparts [2].

Received waveforms always return with some interference which come in four classifications: 1) In all cases, the received waveform will be in the presence of electronic noise that is present in the environment as well as the electronics used in the transmitter and receiver. 2) Often there will be objects not of interest that cause unwanted reflections back to the receiver that are known as *clutter*. 3) In today's

world of wireless technology, the atmosphere is filled with electromagnetic radiation from human-made sources which can cause unwanted electromagnetic interference. 4) In military applications, intentional jamming in the form of noise or false targets due to electronic countermeasures is often present. Radar receivers need to be able to perform in the presence of each of these types of interference [2].

The circuits discussed in this dissertation deal with determing two measurements from the received radar pulse – target range and velocity. Because radar uses electromagnetic waves that travel at the speed light, the range R to an object can be determined by

$$R = \frac{c \times \Delta T}{2} \tag{1.1}$$

where c is the speed of light which is approximately 3×10^8 m/s and ΔT is the delay between transmission and reception.

When an electromagnetic wave reflects off of a moving object, it will undergo a shift in frequency propertional to the target's velocity known as a Doppler shift. The Doppler shift can be calculated to be

$$f_D \cong \frac{2 \times v}{\lambda} \tag{1.2}$$

where v is the target's velocity and λ is the wavelength of the transmitted electromagnetic waveform.

1.2 A Pulsed-Doppler Radar System

In a pulsed-Doppler radar system, radio frequency (RF) pulses are transmitted, and the Doppler shifted echo signal is returned and processed by the receiver. An example of a pulsed-Doppler radar system [3] is shown in Figure 1.2. This system aims to measure the range and velocity of a target by detecting the transmit time

and Doppler shift of a reflected RF modulated pulse.

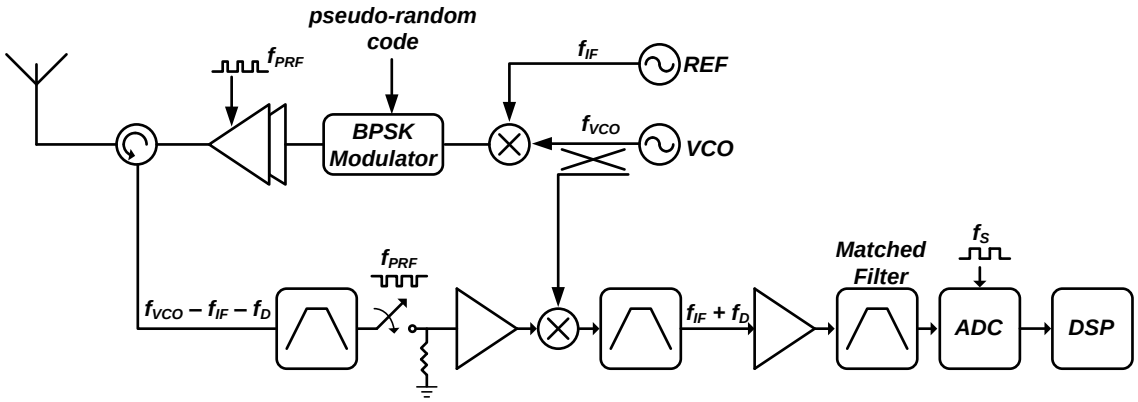


Figure 1.2: Block diagram of a pulsed-Doppler radar system with monobit subsampling.

The transmitter path of Figure 1.2 consists of a pair of signal sources – a reference oscillator operating at the intermediate frequency (IF) f_{IF} and a voltage-controlled oscillator (VCO) operating at the RF frequency f_{VCO}. The reference signal is up-converted to $f_{VCO} - f_{IF}$ and then pulse modulated at a pulse repetition frequency (PRF) f_{PRF}. A pseudorandom Binary Phase Shift Keying (BPSK) phase code of either 0° or 180° is employed to eliminate any range ambiguities that may be present while also reducing the receiver sensitivity to any in-band interferers that may be present. The BPSK modulated, pulsed, RF signal is radiated from the antenna to the target and then reflected back to the antenna with some delay proportionate to the distance between antenna and target. The return signal also undergoes a Doppler shift f_D dependent on the target's velocity. The received signal at $f_{VCO} - f_{IF} - f_D$ is amplified, bandpass filtered, and then down-converted by an image-reject mixer to $f_{IF} + f_D$. This IF signal is bandpass filtered through a radar matched filter and

then sampled once per pulse by a 1-bit ADC clocked at $f_S = f_{PRF}$. The sampled signal is then processed by a digital signal processor (DSP) for analysis to determine the range and velocity of the target.

In these systems, the received signals are typically very weak, often much weaker than the surrounding noise levels resulting in poor signal-to-noise (SNR) ratios. In designing the matched filter, it would be beneficial to reduce the bandwidth as much as possible in order to maximize the SNR at the input to the ADC; however, filter bandwidths that are too small would not be able to pass the received pulse without significant distortion of the pulse shape in the time domain. Therefore, the matched filter must be designed with a sufficiently large enough bandwidth to pass the received pulse without causing extreme time-domain distortion while still being sufficiently small in bandwidth in order to maximize receiver SNR. Since the transmitted RF pulse width varies depending on the distance of the object, it is desirable to have a filter with a tunable bandwidth to operate optimally at varying pulse widths; thus, a"matched filter" is designed since its bandwidth is related to the transmitted pulse width.

In current applications, the matched filter has typically been implemented with SAW and BAW filters. The disadvantage of these filters is that they are bulky, not tunable, temperature sensitive, and must be off chip which is expensive compared to on-chip solutions. In order to be programmable, several of these filters need to be used with complex switching networks. In this dissertation, a novel matched filter design is proposed which is both highly tunable and implementable on a single integrated circuit chip.

Following the matched filter is a subsampling ADC. Due to the received signal typically being of low SNR, having a large resolution ADC is not required since thermal noise will likely be larger than the quantization noise. Because of this a

mono-bit ADC is used which is simpler and requires less silicon area than its multi-bit counterparts.

The output of the ADC is passed to a DSP in order to demodulate the filtered BPSK pulse and recover the Doppler frequency. Typically, the DSP uses averaging techniques to help improve the SNR of the signal. This dissertation proposes a new method of using a simple delta-sigma ($\Delta\Sigma$) modulator with an additional set of switches to demodulate the filtered BPSK pulse and recover the Doppler tone while improving the output SNR without any additional averaging by the DSP.

1.3 Organization of This Dissertation

The remainder of this dissertation is organized as follows. In Chapter 2, a G_m-C filter is proposed that is implemented using differential difference amplifers (DDAs). This filter acts as an anti-aliasing filter to attenuate out-of-band components before they are processed by the following FIR filter. The implementation using DDAs shows that the power consumption of the filter can be greatly reduced when compared to previously reported designs.

Chapter 3 presents a novel matched filter design based on a finite impulse response (FIR) structure. Due to the filter structure being of an FIR design, constant group delay is achieved by proper selection of the filter's coefficients. The filter's transfer function is made tunable by using a novel transconductor tuning scheme which allows the FIR transfer function coefficients to be easily modifiable. This allows for the filter bandwidth to be adjusted to the optimal value for varying transmitter pulse widths.

Chapter 4 presents a correlation based coherent digitizer that is based on a $\Delta\Sigma$ modulator which demodulates the filtered BPSK pulse at the output of the matched filter and recovers the Doppler frequency information. The demodulation of the BPSK signal effectively reduces the signal bandwidth which allows an improvement in

SNR when the out-of-band thermal noise is filtered by the DSP. Additional averaging is not required to recover the Doppler frequency information which reduces post-processing complexity.

Finally, Chapter 5 offers concluding remarks and recommendations for possible future work.

2. LOW-POWER G_M-C FILTER EMPLOYING CURRENT-REUSE DIFFERENTIAL DIFFERENCE AMPLIFIERS

In the following chapter, a matched filter for pulsed-Doppler radar systems will be presented. This filter uses a discrete time FIR filter which is tunable in bandwidth. Because of the discrete time operation of the filter, the input must be sampled with a sample-and-hold in order to discretize the signal in the time domain. According to the the Nyquist sampling theorem, in order to avoid aliasing the sampling frequency should be at least twice the maximum frequency contained in the signal, or

$$f_S > 2 \times f_{max}. \tag{2.1}$$

This means that the spectrum of the signal should be zero above $f_S/2$. If this requirement is not met, the spectral content above $f_S/2$ will fold back in-band which will distort the desired signal causing an irreversible loss of information.

In the FIR filter discussed in Chapter 3, the input signal is sampled at a clock rate of 150 MHz. In this chapter, an anti-alias filter is presented which will attenuate the spectral content above $f_S/2$ in order to eliminate as much as possible the alias effect.

2.1 Anti-Alias Filter Requirements

Figure 2.1 shows a discrete-time bandpass filter frequency response similar to that of the FIR filter which will be presented in the next chapter. The sample rate is 150 MHz, therefore spectral content beyond $f_S/2$, or 75 MHz will alias back to baseband. When the FIR filter is set to have a 30 MHz bandwidth, the maximum in-band frequency will be 55 MHz since the IF is 40 MHz. Due to the sampling,

spectral content from 95 to 125 MHz will alias back into the FIR filter's passband of 25 to 55 MHz. To avoid loss of information, an anti-alias filter needs to be used to suppress this higher frequency content.

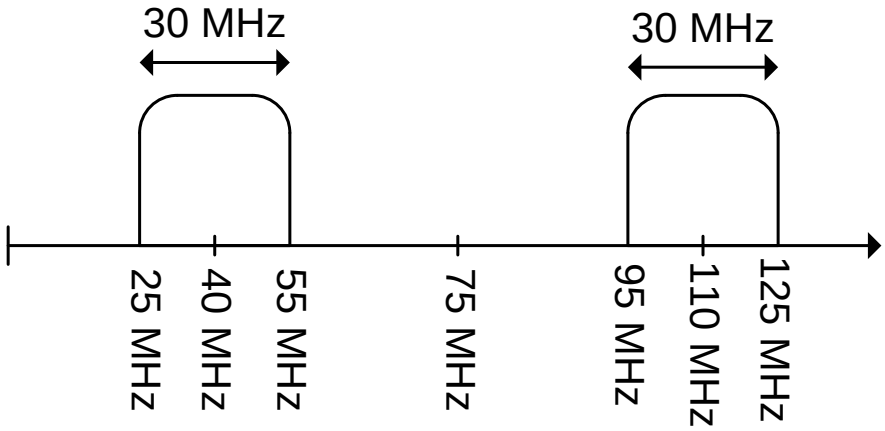


Figure 2.1: FIR filter main spectrum and first image which will alias back in-band.

The anti-alias filter should have a cutoff frequency just beyond 55 MHz and provide as much attenuation as possible before 95 MHz. It should also have minimal group delay variations in order to not cause time-domain skewing in the pulse envelope. A 6th order Butterworth filter was chosen as a compromise between attenuation rate and group delay variation. The cutoff frequency of 65 MHz was set slightly beyond the FIR filter corner in order to not disturb the FIR filter transfer function at the transition area. Table 2.1 lists the ω_0 and Q values needed for the 6th order filter. The ideal magnitude response is shown in Figure 2.2. There is -15 dB attenuation at 95 MHz where the first alias components start to appear. In order to have 40 dB attenuation at 95 MHz, the filter would need to be 16th order which was not practical in this design due to silicon area constraints.

Table 2.1: ω_0 and Q values for anti-alias filter.

	Stage 1	Stage 2	Stage 3
ω_0	4.4922×10^8	4.4922×10^8	4.4922×10^8
Q	0.5176	0.7071	1.9321

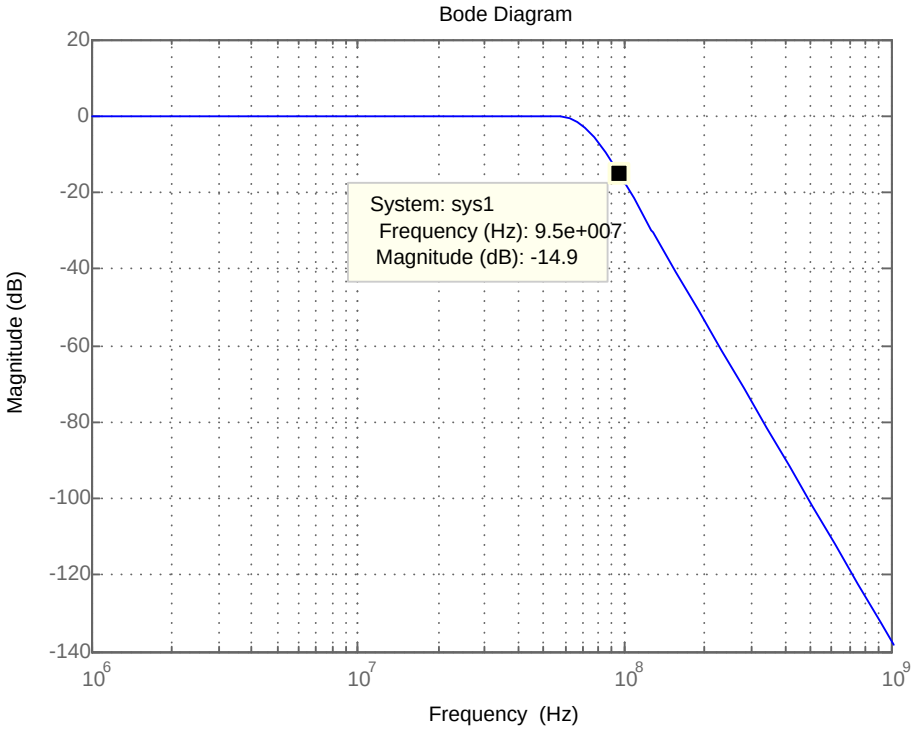


Figure 2.2: Ideal magnitude response of 6th order Butterworth filter.

2.2 Filter Architecture Selection

For high frequency bandwidths, G_m-C filters are preferred for medium linearity applications [4]. One of the main disadvantages of G_m-C filters is their limited linearity; because each amplifier operates in open loop, large voltage swing appears at each amplifier input. Several techniques have been reported to improve the linearity of the OTA [5–9]. In almost all of the G_m-C implementations, the focus is put only

into the OTA cell to improve the linearity; little innovation is typically done in the system level architecture of the filter to reduce the noise or power consumption.

For medium resolution Nyquist rate ADCs (8 bits or less), usually power consumption and noise performance are more critical design parameters than linearity; this is the target of the proposed filter's approach. In this chapter, a current re-use system level architecture based on differential difference amplifiers (DDA) is proposed that reduces the power consumption by half and reduces the thermal noise. Two independent OTAs re-use the same DC current by having similar operation as the differential difference architectures while consuming fifty percent less power and having less thermal noise than conventional approaches.

2.3 Continuous-Time Filters Employing Differential-Difference Amplifiers

The differential-difference amplifier was first suggested in [10] as a versatile building block offering a pair of differential inputs sharing the same output (dual-input, single-output). The availability of multiple inputs makes this analog block attractive for a number of applications such as filters [11], amplifiers [12], common-mode feedback circuits [13, 14], and input stages of fast comparators needed in a variety of analog-to-digital converters [15]. The simplified schematic of the single-stage fully-differential architecture is depicted in Figure 2.3. Two differential pairs process the differential input signals with the drains of each differential pair being connected at the output leading to the differential output current given by

$$i_{out} = i_{o1} - i_{o2} = G_{m1}\left(v_{i2} - v_{i1}\right) + G_{m2}\left(v_{i4} - v_{i3}\right) \tag{2.2}$$

where G_{mi} is the small signal transconductance of the transistors M_i determined by the bias current and transistor dimensions.

Major drawbacks to OTA-C filters, including realizations with DDAs, are i) the

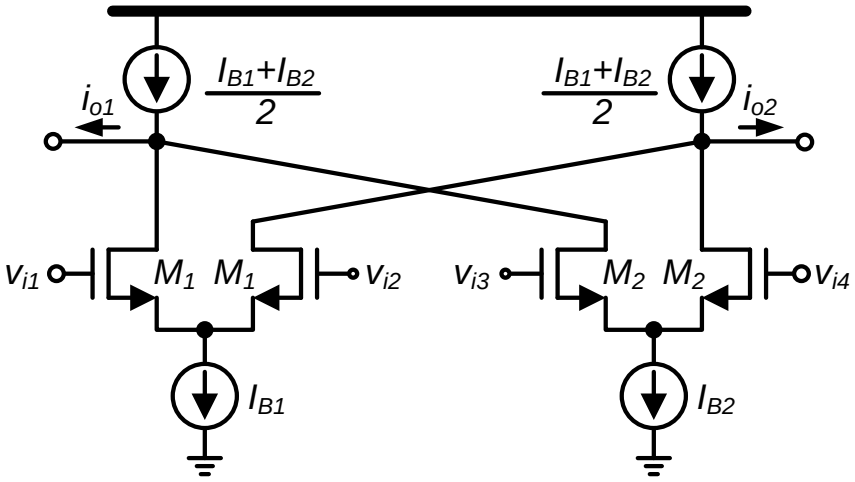


Figure 2.3: Single-stage differential difference amplifier.

significant noise contribution of the current sources used to compensate the DC current needed at the drain of the transistors; notice that the differential output referred current noise density due to these current sources is approximately equal to $8kT\gamma G_{mp}$ A^2/Hz with the bias current source being equal to $0.5(I_{B1} + I_{B2})$ and G_{mp} being the transconductance of the bias current source transistors; ii) the power efficiency of the OTA-C architecture is poor. The maximum AC voltage swing is limited by the linearity requirements which usually limit the signal magnitude to be less than the overdrive voltage of the transistors of the differential pairs; therefore, the voltage efficiency, defined here as the ratio of the peak value of the signal to the supply voltage, is usually small; e.g. less than 20 percent for medium linearity applications. With the aim of having first order results, consider the case of a single stage OTA employing a differential pair. First order estimation of the third order harmonic distortion HD_3 leads to the following result for long channel devices [4]:

$$HD_3 \cong \frac{1}{32}\left(\frac{v_{in}}{V_{DSAT}}\right)^2 \tag{2.3}$$

where v_{in} is the amplitude of the input signal and V_{DSAT} is the transistor's overdrive voltage. Thus for $HD_3 < -40$ dB, the ratio of the input signal amplitude to the overdive voltage is limited to $v_{in}/V_{DSAT} < 0.5$. Assuming the quadratic model for long-channel devices and (2.3), the OTA power efficiency PE can be obtained as

$$\begin{aligned} PE &= \left(\frac{v_{in}}{V_{DD}}\right)\left(\frac{i_O}{I_B}\right) \\ &= \left(\frac{v_{in}}{V_{DD}}\right)\left(\frac{G_m v_{in}}{I_B}\right) \\ &= \left(\frac{V_{DSAT}}{V_{DD}}\right) \times 64 \times HD_3. \end{aligned} \tag{2.4}$$

According to (2.4), the OTA PE is around 10 percent for the case of $HD_3 = -40$ dB (=0.01) and $V_{DSAT}/V_{DD} = 0.3/1.8$, but only 1 percent for the case of $HD_3 = -60$ dB.

Source degeneration and other linearization techniques improve the voltage efficiency at the expense of a decrement in both current efficiency and voltage gain as well as an increase in noise level. Unfortunately, large source degeneration factors might not be feasible for advanced technologies where the power supplies are limited. On the other hand, current re-use techniques improve the OTA power efficiency since the same bias current is used for multiple purposes. In the next section, a current re-use biquad based on a DDA will be introduced.

2.4 Current Reused G_m Cells for Biquadratic Filters

One of the main issues of a biquad filter is that each implemented OTA is power hungry and noisy. Most of the research on biquad filters is focused on optimizing the design of the OTA by improving the linearity and attempting to reduce the power consumption; however, as predicted by (2.4), design tradeoffs limit its power efficiency.

In G_m-C filter realizations such as the biquad shown in Figure 2.4, each of the OTAs is comprised of a voltage-to-current converter usually based on a conventional differential pair (CDP) as shown in Figure 2.5a. The N-type CDP realizes the voltage-to-current conversion while the P-type transistors are used as current sources to bias the arms of the CDP. Even if the CDP is an efficient voltage-to-current converter, the power dissipated by the P-type transistors is not used for signal processing thus reducing the circuit's power efficiency; the noise introduced by the P-type transistors also reduces the OTA's signal-to-noise ratio.

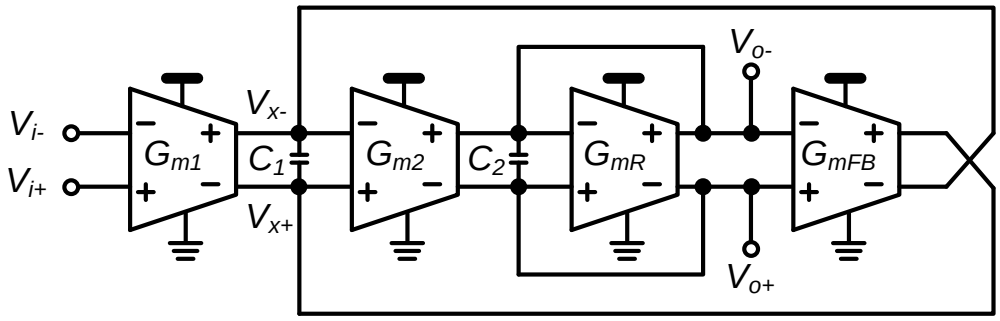


Figure 2.4: Typical implementation of a G_m-C biquad filter.

In Figure 2.5b, the complimentary dual differential pair (DDP) based transconductor which employs both N- and P-type differential pairs is shown. If the DDP is designed to have the same transconductance as the CDP of Figure 2.5a, and assuming that each differential pair provides equal transconductance, the current of the DDP can be halved. The output noise current is reduced from the CDP case since both of the noise contributors are halved. One downside is that the input capacitance increases.

The current-reused DDA topology is shown in Figure 2.5c. This topology uses the same amount of current as the CDP to produce the desired transconductance;

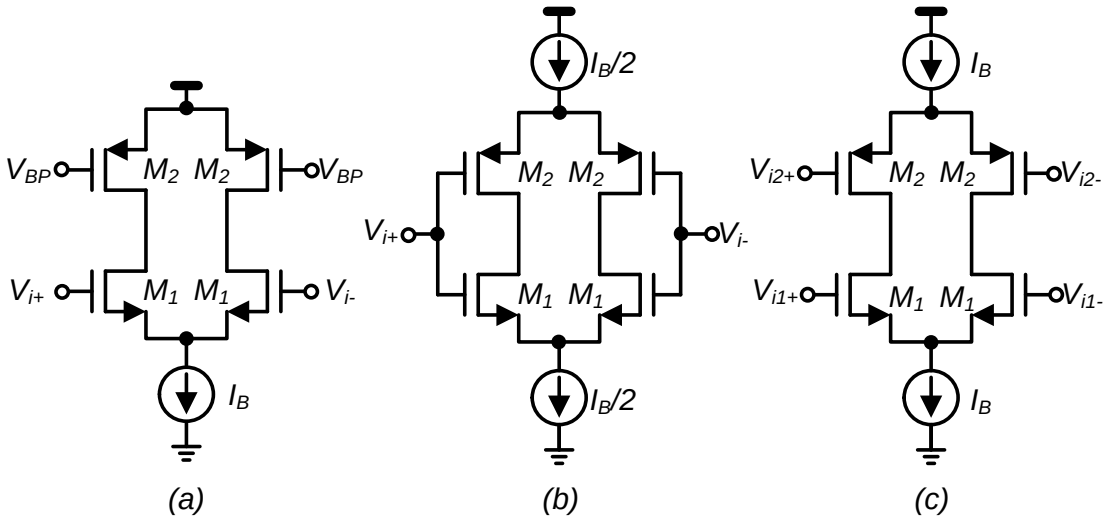


Figure 2.5: (a) Conventional differential pair, (b) dual differential pair using half the bias current, and (c) current-reuse differential difference amplifier.

however, the P-type transistors are arranged to produce a second transconductance which can be used in the biquad filter to make it more efficient. The DDA topology produces two transconductors for the same bias current as the CDP therefore reducing the average power per OTA by half.

Table 2.2 compares the various performance metrics of the three topologies. For this table, it is assumed that the overdrive voltage is maintained constant for all transistors. The CDP employs two bias currents which contribute to 50 percent of the power and noise but not to signal power. The DDP topology is more efficient in terms of power due to the bias current being reused which results in a 50 percent reduction in power consumption for the same transconductance gain compared to the conventional differential pair case. Input capacitance for the DDP OTA approximately doubles compared to the CDP since μ_n is approximately three times μ_p for modern technologies and C_{gs1} is around 50 percent of that of the conventional architecture due to the reduced bias current used. Even though the output noise

Table 2.2: Performance comparison between the conventional differential pair, dual differential pair, and proposed current reuse topology.

Metric	Conventional	DDP	Current Re-use DDA
Transconductance per OTA	$G_m = g_{m1}$	$G_m = g_{m3} + g_{m4} = \frac{g_{m1}+g_{m2}}{2}$	$G_m = g_{m5}, g_{m6} = g_{m1}, g_{m2}$
Bias current per OTA	I_B	$I_B/2$	$I_B/2$ (average per OTA)
Noise density per 2 OTAs	$16kT(g_{m1} + g_{m2})$	$8kT(g_{m1} + g_{m2})$	$8kT(g_{m1} + g_{m2})$
Input capacitance per OTA	C_{gs1}	$\frac{C_{gs1}}{2}\left(1 + \frac{\mu_n}{\mu_p}\right)$	C_{gs1};$C_{gs1}\left(\frac{\mu_n}{\mu_p}\right)$
Biquad Current	$4I_B$	$2I_B$	$2I_B$

density of the DDP is approximately half that of the DDA, total noise will be approximately equal since two DDPs must be used for the same functionality as the DDA architecture. For the DDA architecture, the input capacitance for the biquad filter is similar to the CDP if the N-type differential pair is used. In the proposed biquadratic filter, the small capacitance N-type differential pair is used as the input stage to reduce loading in the preceding stage, while the P-type differential pairs with larger capacitances are used for internal filter nodes where the capacitance can easily be absorbed.

One drawback of biasing the two differential pairs with the same current is that design freedom becomes limited. If the bias current is set to provide the desired g_m for one of the differential pairs, only the transistor dimensions can be changed for the second differential pair which affects linear range. This drawback is somewhat alleviated by adding source degeneration resistors which give an extra design variable as shown in the following section.

2.5 DDA Based Biquad Filter Circuit Implementation

The transistor level schematic of the implemented current reused biquad is shown in Figure 2.6. A differential pair with source degeneration is used to implement the OTA. Since linearity is relaxed in this application, no additional linearization techniques are used because they would likely increase power consumption and hinder noise performance. The NMOS input OTA is biased with a PMOS differential pair with source degeneration which acts as the feedback OTA from Figure 2.4. The design uses a split tail-current design in order to not encounter the voltage drop across the source degeneration resistors which was found not to be feasible due to limited voltage headroom. Unfortunately the noise of the bias current source I_{B1} contributes the differential OTA output noise; this drawback, however, may not

be very significant as demonstrated in the following section. The full biquad filter of Figure 2.4 was implemented using two DDAs with the PMOS inputs receiving the output from the opposite DDA. The second N-type differential pair realizes the biquad lossy element that determines the filters Q-factor.

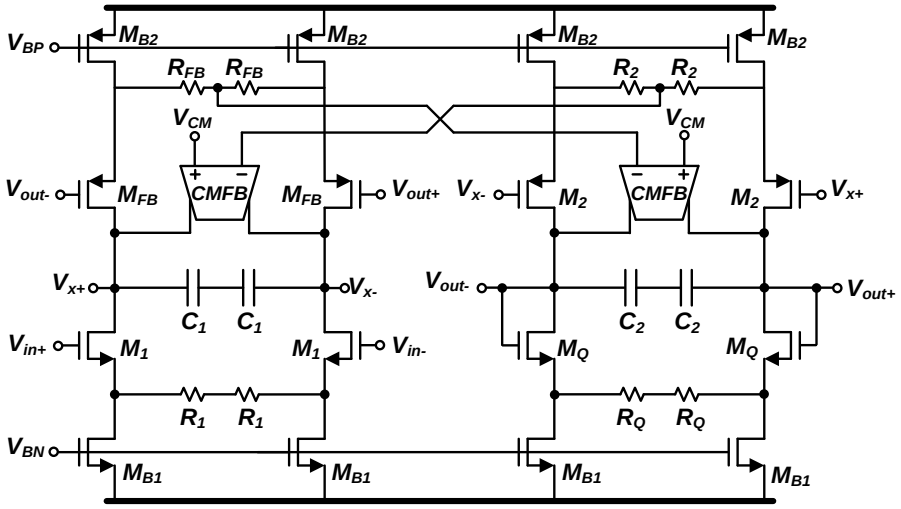


Figure 2.6: Transistor level implementation of proposed current-reused G_m-C biquad.

The transfer function of the implemented circuit is equal to the classical biquad circuit implementation of Figure 2.4

$$H(s) = \frac{\frac{G_{m1}G_{m2}}{C_1C_2}}{s^2 + s\frac{G_{mR}}{C_1} + \frac{G_{m2}G_{mFB}}{C_1C_2}} \tag{2.5}$$

where G_{mi} is the overall transconductance gain of the i_{th} source-degenerated differential pair and are calculated as

$$G_{m1} = \frac{g_{m1}}{1 + g_{m1}R_1} \tag{2.6}$$

$$G_{m2} = \frac{g_{m2}}{1 + g_{m2}R_2} \tag{2.7}$$

$$G_{mR} = \frac{g_{m,Q}}{1 + g_{mQ}R_Q} \tag{2.8}$$

$$G_{mFB} = \frac{g_{m,FB}}{1 + g_{m,FB}R_{FB}} \tag{2.9}$$

The common-mode detector needed for the common-mode feedback (CMFB) is non-invasive to the output avoiding extra resistive loading that can reduce the gain of the OTAs and limit their bandwidth due to extra parasitic capactiance. The realization of the CMFB amplifier is discussed in the following subsections.

Table 2.3 lists the sizes of the transistors used in the biquad filter. All three biquad filters used the same tranistor sizes in order to simplify the design. The source degeneration resistors were modified between stages to tune the transconductances to the needed value. Table 2.4 lists the sizes of the source degeneration resistors that were used.

Table 2.3: Biquad filter transistor sizes.

Transistor	Size (μm/μm)
M_1, M_Q	175/0.36
M_2, M_{FB}, M_{B2}	126/0.18
M_{B1}	84/0.36

2.5.1 Power Efficiency

The primary benefit of the proposed current-reused biquad is reduced current consumption which will double the power efficiency of the proposed topology if the voltage swing can be accommodated without increasing the power supply. In principle, the voltage swing can be as large as the threshold voltage V_{TH} of the transistors

Table 2.4: Biquad filter source degeneration resistor values.

Component	Biquad 1	Biquad 2	Biquad 3
R_1	24 kΩ	800 Ω	2.3 kΩ
R_2	1.6 kΩ	720 Ω	720 Ω
R_{FB}	1.6 kΩ	4.4 kΩ	4.4 kΩ
R_{RQ}	1.5 kΩ	1.4 kΩ	7 kΩ

if the OTA's input and output signals are around 90 degrees out-of-phase, but signal swing could be limited to $V_{TH}/2$ if they are around 180 degrees out-of-phase. Fortunately, in the case of filters with low Q (less than 1), the signal swing at the filter's internal nodes is less than or equal to the signal swing at the input which alleviates these issues. Also, in filters such as the one shown in Figure 2.4, the node V_x is approximately 90 degrees out-of-phase with respect the input and output signals which helps to avoid signal saturation.

2.5.2 Noise

It is well known that the reduction of input referred noise comes with the penalty of more power consumption and larger area since thermal noise is inversely proportional to capacitance. The DDA implementation in this design reduces the input referred noise without the need of additional power or increasing the area. In order to have a fair comparison in the noise performance of a biquad filter using DDAs and one using current-source loaded differential pairs, it is useful to look at the noise performance of just a single OTA in the system. Figure 2.7 shows the included noise sources for one of the OTAs in the DDA current-reused topology. Only the NMOS transistors with their noise sources are included because the PMOS transistors are all used to create a separate transconductor. The differential input referred noise of the transconductor is given by (2.10) where g_{mB1} is the transconductance of the

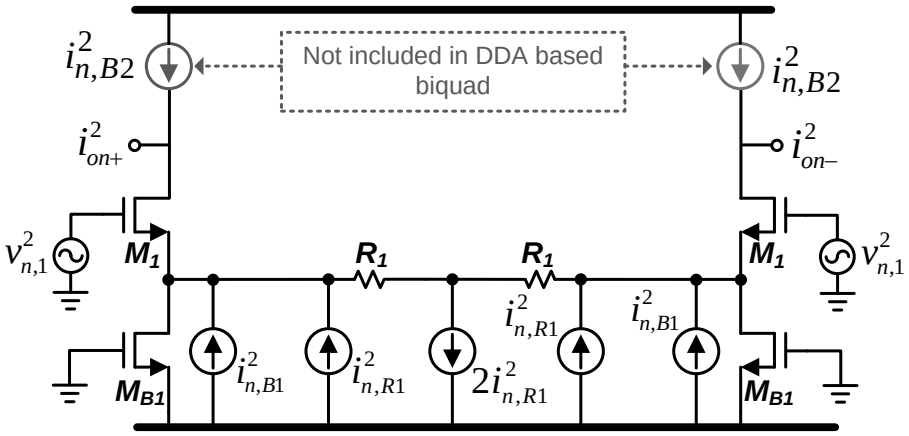


Figure 2.7: Noise sources for a single transconductor in the proposed DDA topology.

bias transistor M_{B1} and N_R is the source degeneration factor $g_{m1}R_1$. To compare the noise to that of a current source loaded differential pair with source degeneration using the same split tail current topology, the input referred noise can be derived as in (2.11) where the only difference is the right-most term in the bracket which is the noise from the bias current source.

$$V^2_{n,i,DDA} = \frac{8kT}{g_{m1}}\left(\gamma + N_R + \frac{\gamma g_{mB1} N_R^2}{g_{m1}}\right) \tag{2.10}$$

$$V^2_{n,i,conventional} = \frac{8kT}{g_{m1}}\left(\gamma + N_R + \frac{\gamma g_{mB1} N_R^2}{g_{m1}} + \frac{\gamma g_{mB2}\left(1+N_R\right)^2}{g_{m1}}\right) \tag{2.11}$$

As shown in (2.10) and (2.11), the proposed topology will reduce the input referred noise of the filter. As previously mentioned, it was necessary to split the tail current source in order to alleviate the voltage drop on the source degeneration resistor since the input common-mode voltage needs to be in the middle of the supply rails. For a current-source loaded OTA, it would be possible to raise the input common-mode voltage which would allow the tail current to be placed be-

tween the source-degeneration resistors. In this case, the noise from the tail current source would only be common-mode noise (ignoring differential mode noise due to mismatch) which would set the third term in the parenthesis in (2.11) to zero; the noise would thus be approximately equal to that of (2.10), the DDA case.

The filter was simulated in Cadence to test the noise performance. Figure 2.8 shows the input noise spectral density in the FIR filter's passband range of 25 to 55 MHz. The noise spectral density is approximately 40 nV/Hz$^{1/2}$ which is comparable to previously published results [6,7]. Integrated across the 30 MHz bandwidth of the maximum bandwidth of the matched filter, the total noise is 48 nV which is around 61 dB SNR for a 0 dBm input power. This result is better than the following sample-and-hold, therefore it will have negligble effect on the total SNR of the system.

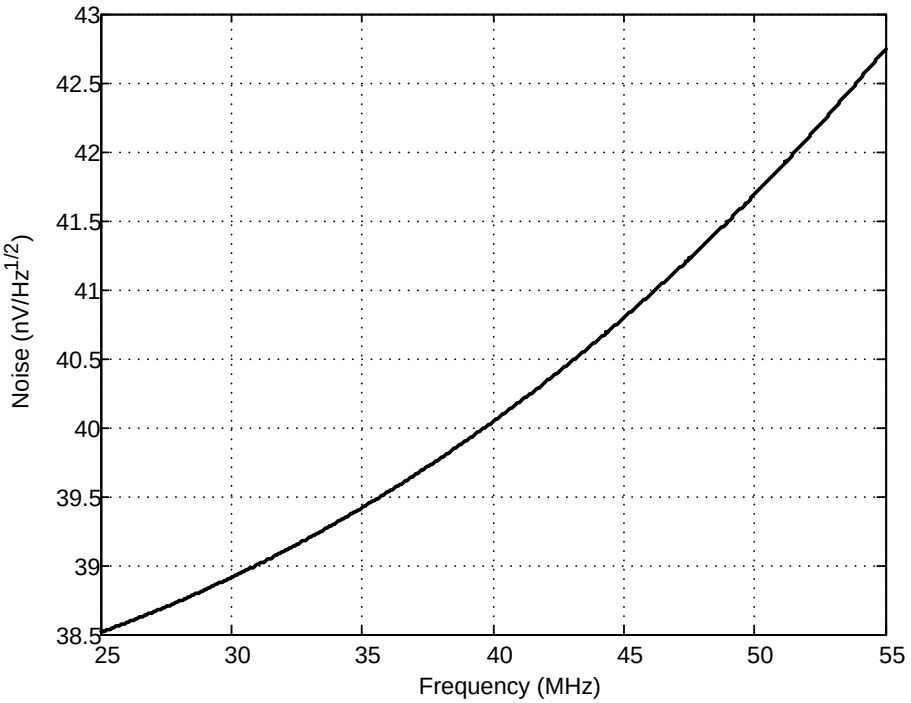


Figure 2.8: Input referred noise spectral density for anti-alias filter.

2.5.3 Common-Mode Feedback

In order to reduce Q variations, high gain from the OTA is desired. Figure 2.9 shows an example of the classical way CMFB is employed [16]. The two resistors R_{CMFB} at the output sense the output common-mode voltage $V_{CM,out}$ which is then compared to a reference voltage $V_{CM,ref}$ which is the desired common-mode output. This creates a control voltage V_{CMFB} which is fed back to the amplifier to adjust the output common-mode level. Because the two sense resistors are at the output node, they will be in parallel with the amplifier's output resistance which causes a reduction in gain.

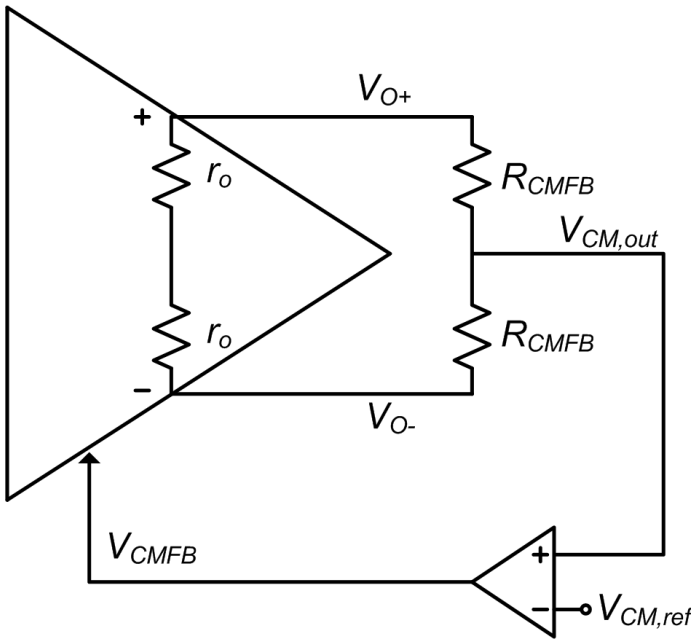


Figure 2.9: Classical CMFB topology which loads the amplifier output causing a reduction in gain.

As shown in Figure 2.6, the implemented CMFB avoids loading of the output nodes by sensing the common-mode voltage from the node between the source degen-

eration resistors, albeit with a DC level shift. The implemented OTA to compensate for common-mode variations is shown in Figure 2.10a which is based on the topology presented in [17] with the capacitor C_{cm1} added. The small signal model of one of the two common-mode loops is illustrated in Figure 2.11. Without the compensation network consisting of R_{cm}, C_{cm1}, and C_{cm2}, there are three parasitic poles which are given by

$$\omega_{p1} = -\frac{1}{R_{o1}C_{p2}} \tag{2.12}$$

$$\omega_{p2} = -\frac{1}{R_{o2}C_{p3}} \tag{2.13}$$

$$\omega_{p3} = -\frac{1}{R_{sd}C_{p1}} \tag{2.14}$$

where C_{pi} is the parasitic capacitance at each respective node, R_{o1} and R_{o2} are the output resistances of the two amplification stages, and R_{sd} is the source-degeneration resistance from Figure 2.6 used to detect the common-mode signal.

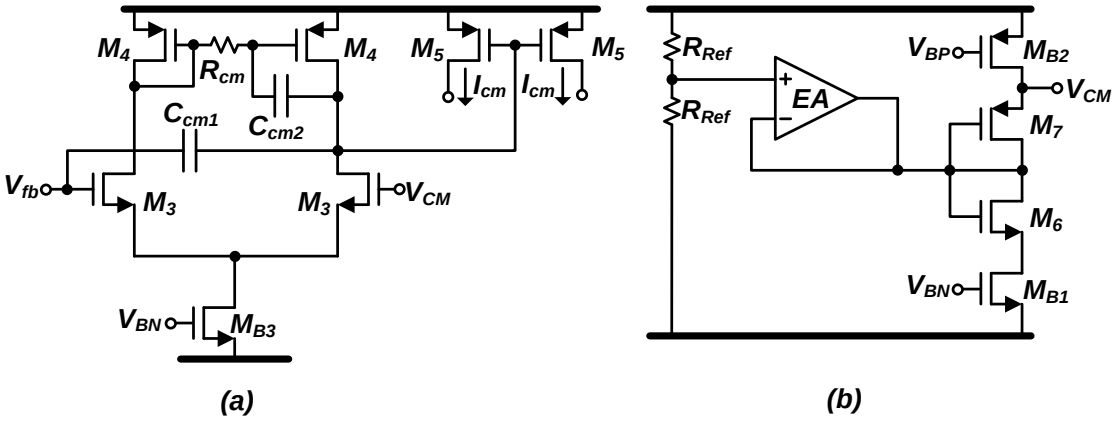


Figure 2.10: (a) Proposed common-mode feedback circuit with (b) replica circuit for proper generation of common-mode voltage reference V_{CM}.

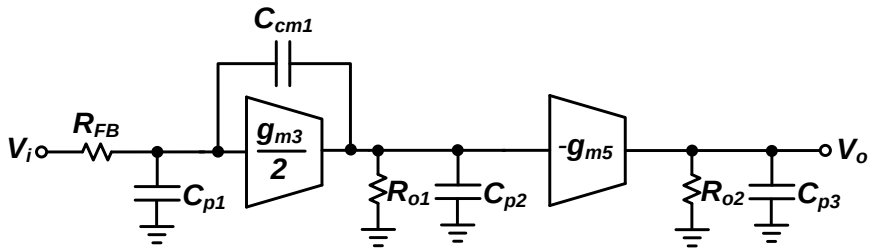


Figure 2.11: Small signal model of common-mode loop for one of the two common-mode loops.

The location of these parasitic poles is illustrated in the s-plane diagram of Figure 2.12a. While ω_{p3} is located well beyond the unity gain frequency, ω_{p1} and ω_{p2} are located very near each other which will result in poor phase performance.

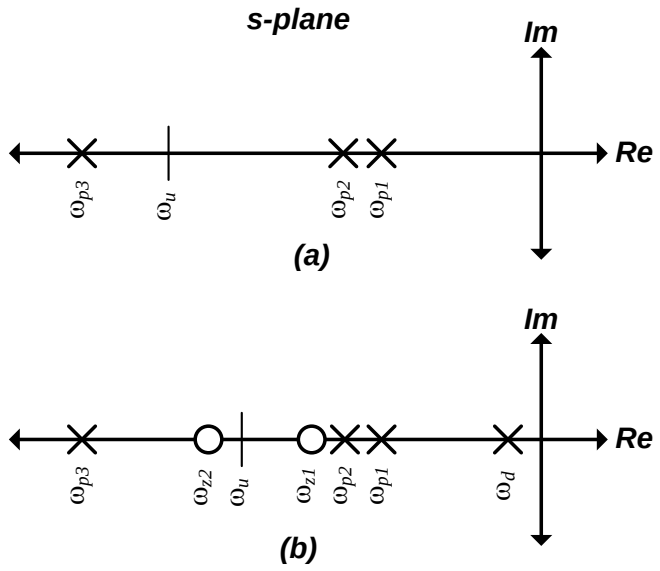


Figure 2.12: Pole-zero plot for the CMFB loop when the circuit is (a) uncompensated and (b) compensated.

Due to the multiple poles in the loop, the compensation structure involving R_{cm},

C_{cm1}, and C_{cm2} were added. By adding the compensation network, the loop gain can be derived as in (2.15)-(2.19)

$$H_{CM}(s) \approx H_0 \frac{(1+s/\omega_{z1})(1+s/\omega_{z2})}{(1+s/\omega_d)(1+s/\omega_{p1})(1+s/\omega_{p2})(1+s/\omega_{p3})} \tag{2.15}$$

$$H_0 = g_{m3} g_{m5} R_{o1} R_{o2} \tag{2.16}$$

$$\omega_{z1} = -\frac{2}{\left(R_{cm} - \frac{1}{g_{m4}}\right) C_{cm2}} \tag{2.17}$$

$$\omega_{z2} = -\frac{g_{m3}}{2C_{cm1}} \tag{2.18}$$

$$\omega_d = -\frac{1}{g_{m4} R_{o1} R_{cm} C_{cm2}} \tag{2.19}$$

where ω_{p1}, ω_{p2}, and ω_{p3} are the same as the uncompensated case.

The s-plane representation of the compensated system is illustrated in Figure 2.12b. Because of the Miller effect, the dominant pole ω_d is controlled with R_{cm} and C_{cm2}. If R_{cm} is made large enough, i.e. greater than $1/g_{m4}$, the zero introduced through this network is pushed into the left-hand plane which helps to further stabilize the system. In this design, this zero was placed near ω_{p1} and ω_{p2}. To further improve the stability, C_{cm1} is added which will introduce another left-hand plane zero which can be placed near the unity gain frequency to provide a boost in phase margin. Notice that C_{cm1} also introduces a negative capacitance at V_{fb} which further moves the parastic pole at that node to higher frequencies.

The purpose of R_{cm} and C_{cm2} are twofold: i) make transistors M_4 operate as a current mirror to properly bias M_3 while reducing AC signal at medium and high frequencies and ii) C_{cm2} makes the right hand side M_4 transistor operate with its drain-gate connection shorted. This connection results in a low impedance node determined by $1/g_{m4}$ at high frequencies; therefore, the pole at the right hand side

of the M_3 differential pair is shifted to high frequencies to assist with stability.

Since the CMFB amplifier senses the common-mode voltage from the node between the degeneration resistors, the measured DC voltage is not the desired DC voltage for the OTA output as in classical CMFB circuits; instead, it is $V_{CM} + V_{GS,p}$. To force the output DC voltage to the required $V_{DD}/2$, a replica circuit needs to be implemented to generate the required reference voltage. The implemented circuit is shown in Figure 2.10b. A replica circuit of one branch of the proposed current reused biquad is used. Bias transistors M_{b1} and M_{b2} share the same bias circuit as the biquad to ensure that the same DC current is obtained in the replica circuit as the current-reuse OTA. Diode connecting M_2 and forcing its drain to $V_{DD}/2$ by controlling its gate voltage with a local feedback loop is implemented with the error amplifier EA and M_{b3} ensuring an accurate common-mode feedback reference voltage generation. The implementation of the error amplifier is identical to that of the CMFB amplifier of Figure 2.10a except that the transistors M_5 are not included.

Because the sensed common-mode voltage that is fed into the CMFB amplifier has a DC level shift from the true output common-mode voltage, a replica circuit is used to create the appropriate common-mode reference voltage. Figure 2.10b illustrates how the reference voltage for the CMFB amplifier is generated. The error amplifier EA used in the replica circuit is the OTA from Figure 2.10a without the additional transistors M_5.

Transistor sizes for the CMFB network are listed in Table 2.5. The compensation resistor R_{cm} was 15 kΩ while the compensation capacitors C_{cm1} and C_{cm2} were 500 fF and 200 fF, respectively.

Table 2.5: Biquad filter CMFB transistor sizes.

Component	Size (μm/μm)
M_3, M_{B3}	42/0.36
M_4	112/0.36
M_5, M_7, M_{B2}	126/0.18
M_6, M_{B1}	84/0.36
M_8	56/0.18

2.6 Measurement Results

The G_m-C filter was designed and fabricated in 0.18 μm SOI CMOS process by Jazz Semiconductor [18]. Figure 2.13 shows the microphotograph of the fabricated anti-alias filter. The total chip area is 0.21 mm^2.

To measure the frequency response of the filter, the filter was connected to a network analyzer. Figure 2.14 shows the magnitude response of the fabricated filter. The -3 dB corner frequency is approximately 65 MHz. The in-band group delay of the anti-alias filter is shown in Figure 2.15. From 25 MHz to 55 MHz, the maximum passband range of the FIR filter, there is about 3.5 ns total variation in the group delay.

To test the linearity of the filter, two input tones were applied at 39.5 MHz and 40.5 MHz. The power of the two input tones were swept while measuring the total power of the two fundamental tones and two IM3 tones at the output as shown in Figure 2.16. The measured input referred third-order intercept (IIP3) is approximately 12.0 dBm with a 1-dB compression point of 0 dBm. With source degeneration as the only method of linearity improvement and the inclusion of additional current source transistors which limit available voltage headroom, these results are expected.

The results of this work are compared to that of previously published results in

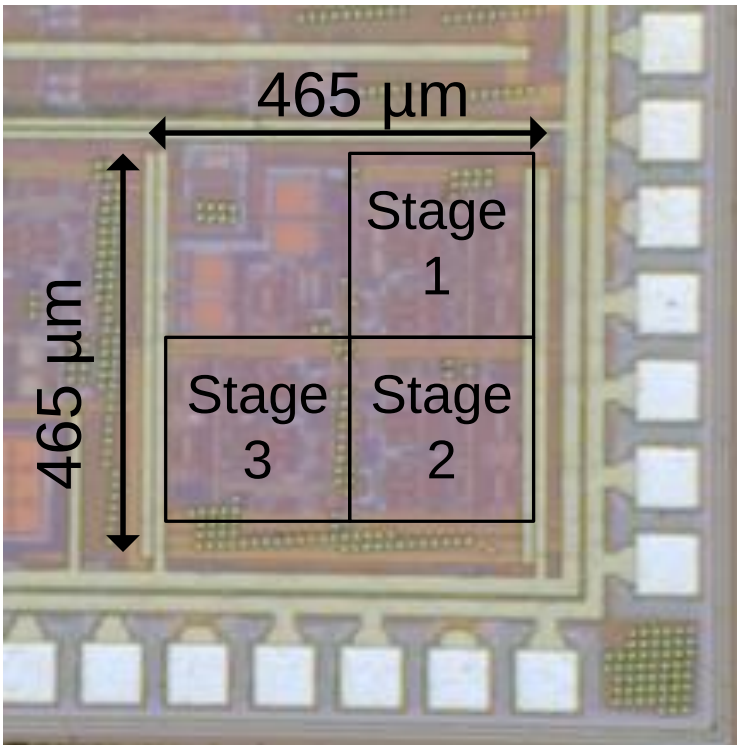


Figure 2.13: Microphotograph of the fabricated low-power G_m-C filter.

Table 2.6 with the Figure of Merrit (FoM) used defined as

$$\text{FoM} = \frac{\text{IIP3} \times \text{f}_{\text{-3dB,MHz}} \times \text{N}}{\text{P}_{\text{mW}}} \tag{2.20}$$

where $\text{f}_{\text{-3dB,MHz}}$ is the -3 dB frequency in MHz, N is the filter order, and P_{mW} is the filter's power consumption in mW. It is seen that this work compares favorably to the state-of-the-art as its FoM greatly exceeds that of the previously published results predominantly because the power per pole in this design is vastly superior.

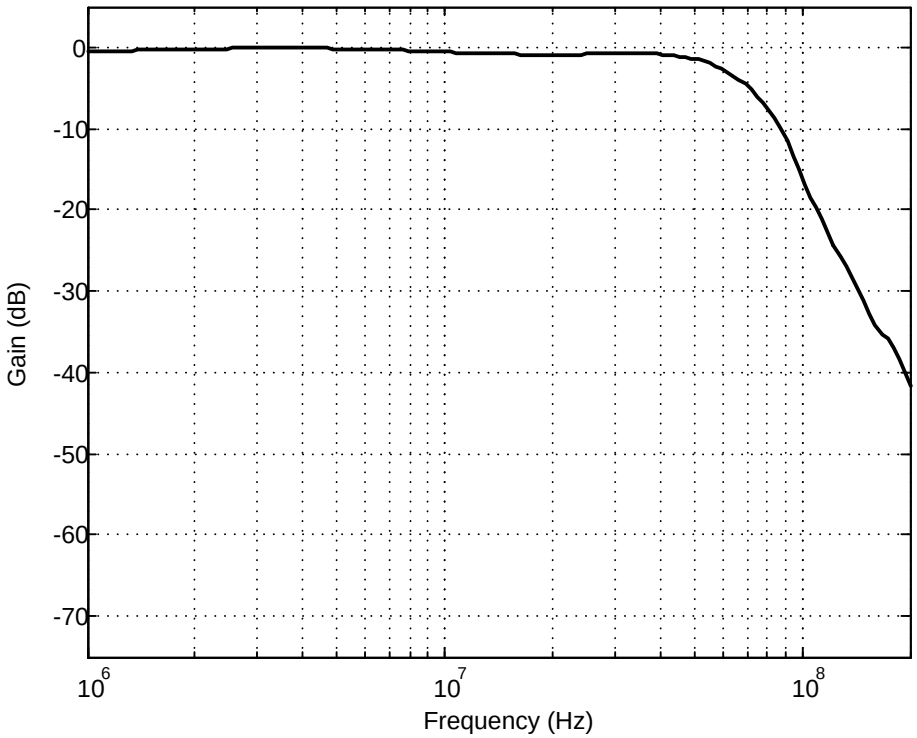


Figure 2.14: Magnitude response of the G_m-C filter.

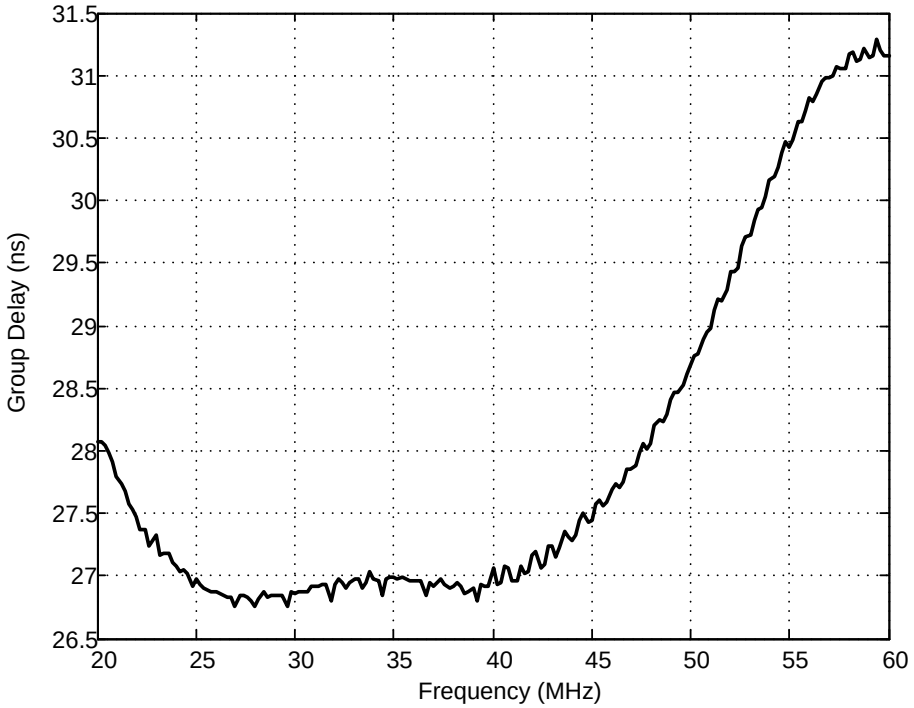


Figure 2.15: In-band group delay of the G_m-C filter.

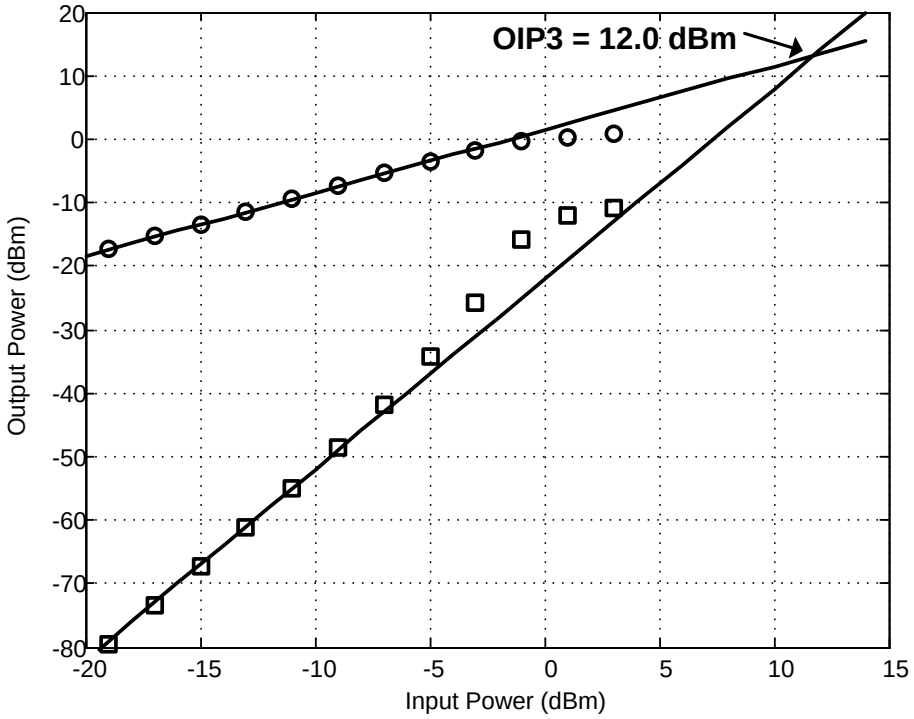


Figure 2.16: Linearity measurement for the G_m-C filter.

Table 2.6: Comparison to previously published results.

Specification	[5]	[6]	[7]	[9]	This Work
Technology (nm)	180	130	350	180	180
Bandwidth (MHz)	50-200	200	200	50-300	65
Filter Order	3	2	7	3	6
Input Noise ($nV/\sqrt{Hz}$)	5	22	65	3	40
IIP3 (dBm)	16	14	11	19	12
Power per Pole (mW)	7.8	10.4	8.6	68.3	1.34
FoM	410	269	256	83	580

2.7 Conclusion

A G_m-C anti-alias filter has been designed for low power applications. Since signal-to-noise-and-distortion ratio (SNDR) for the final application is not critical, the focus of the design was put into power efficiency instead of linearity. The power efficiency was optimized by 50 percent compared to conventional implementations. The architecture was implemented with a current-reuse technique which allows biasing two OTAs with the same DC current. With the implementation of the current-reuse technique, the need of extra bias current sources is avoided. Additionally, the noise performance is improved since fewer transistors will be contributing to the filter's noise. Source degeneration resistors were used to improve the circuit's linearity. The CMFB circuitry measures the common-mode signal from the source degeneration resistors and thus does not load the output of the OTA helping maintain OTA gain. The filter was implemented in Jazz 0.18 μm SOI CMOS and achieves the best power consumption per filter pole compared to previously reported results.

3. A 128-TAP HIGHLY TUNABLE CMOS IF MATCHED FILTER FOR PULSED RADAR APPLICATIONS

In the radar system of Figure 1.2, there is a matched filter which is used to eliminate as much as possible the surrounding thermal noise and blockers that are present in the received signal spectrum. In designing the matched filter, it would be beneficial to reduce the bandwidth as much as possible in order to improve the SNR; however, filter bandwidths that are too narrow would not be able to pass the received pulse without distortion of the pulse envelope in the time-domain. This effect is shown in Figure 3.1. The top waveform in the figure is a 40 MHz input pulsed for 100 ns. When the filter bandwidth is too small, there will be excessive spreading in the time domain. This effect is illustrated in the second waveform which is the case when the filter bandwidth is 3 MHz. Ideally, the filter bandwidth should be approximately the inverse of the pulse width, or 10 MHz in this case. The third waveform shows the case for the 10 MHz bandwidth. The pulse passes without too much spreading in the time domain. The bottom waveform is the case when the bandwidth is wider than necessary, or 30 MHz in this case. There is little difference in the envelope of the 10 MHz and 30 MHz waveforms which means that the filter bandwidth could be reduced in the final case to achieve a better SNR. Therefore the matched filter should be designed with a bandwidth large enough to pass the received pulse without causing extreme time-domain distortion while being narrow enough to maximize receiver SNR.

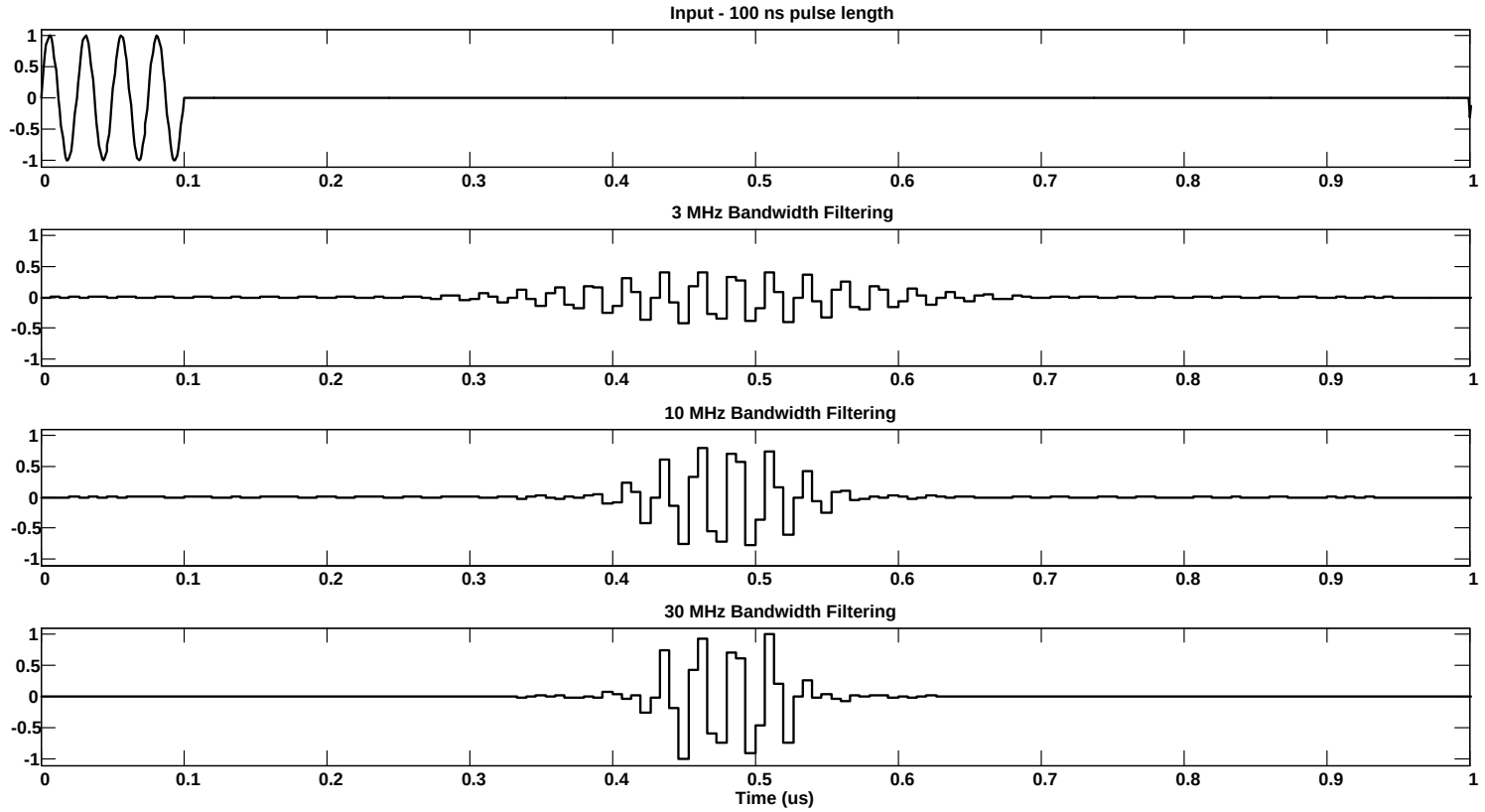


Figure 3.1: Matched filter example with 100 ns pulse time. Top waveform is the input. The second waveform is a filter with 3 MHz bandwidth which is too small for the pulse. The second waveform is the matched filter bandwidth of 10 MHz. The bottom waveform is a 30 MHz bandwidth filter which is excessive.

In current applications, the matched filter has typically been implemented with SAW and BAW filters. The disadvantage of these filters is that they are bulky, untunable, temperature senstive, and must be off chip which is expensive compared to on-chip solutions. In this dissertation, an FIR filter structure is introduced which is widely tunable in bandwidth in order for it to be optimized depending on the pulse width of the transmitted signal.

Most previously reported FIR filters typically fall into one of two categories. References [19–28] all use switched capacitor designs which typically need one amplifier per tap whereas the new trend in research tends toward switched-current techniques [29–46]. Of these, only [39, 40] have reported tunable designs; however, these are lowpass filters which can be adjusted in bandwidth by varying the clock rate. If the transfer functions were modified to a bandpass shape, adjusting the clock rate would not only vary the bandwidth but could also have the unfortunate side effect of varying the filter's center frequency.

In this chapter, an FIR bandpass matched filter design is presented which has a tunable bandwidth from 3 to 30 MHz while being centered at 40 MHz. This filter could potentially replace the SAW or BAW filters that are typically used while moving the filtering function on chip where it can be nearer to the receiver and DSP reducing overall cost. The proposed FIR filter employs 128-taps realized by transconductors, switches, capacitors, and 34 non-overlapping clock phases. The transconductors are highly tunable which allows them to realize various filter bandwidths without modifying the filter's clock rate of 150 MHz. The filter was designed in a Jazz 0.18 μm CMOS SOI process [18] and consumed 450 mW with an attenuation greater than 40 dB at 10 MHz beyond the -3 dB frequency.

3.1 FIR Filter System Level Design

To meet the requirements of the radar receiver, the filter needs to be tunable in bandwidth from 3 to 30 MHz with greater than 40 dB attenuation just 10 MHz beyond the passband while maintaining a linear phase response, i.e. constant group delay. Because this is difficult to achieve with conventional analog filters, a discrete-time FIR topology was chosen. Due to their simplicity, FIR filters can usually be implemented at a much higher order than would be conceivable with G_m-C, active-RC, or switched-capacitor techniques. FIR filters are process, voltage, and temperature (PVT) variation tolerant and usually can be scaled up or down in frequency by scaling the clock frequency. The discrete time FIR filter can have a constant group delay whose value only depends on the clock rate and number of taps.

FIR filters can be described by the equation

$$H(z) = \sum_{n=0}^{N} \alpha_n z^{-n} \tag{3.1}$$

where N is the number of taps. If the coefficients of 3.1 are symmetric, meaning

$$\alpha_n = \alpha_{N-n}, 0 \leq n \leq N, \tag{3.2}$$

then the filter will have linear phase response which provides constant group delay across the frequency band [47]. For the pulsed-Doppler radar filter, constant group delay is desirable because it will allow the received signal to pass the desired intermediate frequency (IF) pulse without causing time-domain distortion in the pulse shape.

MATLAB was used to obtain the required order and coefficients needed for each desired bandwidth. The selected IF was 40 MHz with overall clock rate of 150 MHz.

The bandwidth was tunable from approximately 3 MHz to 30 MHz. In order to obtain the required attenuation of -40 dB at 10 MHz beyond the passband, four identical FIR filters were cascaded as illustrated in Figure 3.2. Since the operation of the FIR filter in this application is discrete-time in nature, the input was first sampled with a sample-and-hold circuit. As will be seen during the discussion of the filter architecture, the input to the filter must remain constant during each clock cycle; therefore, a time-interleaved sample-and-hold topology was used to provide a constant input throughout the entire clock cycle. Using MATLAB, the required FIR filter coefficients α_n were calculated as listed in Table 3.1.

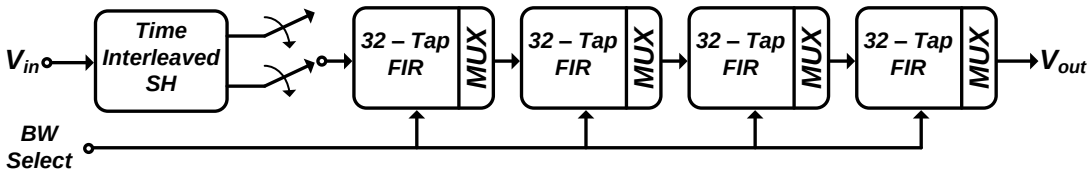


Figure 3.2: Proposed 128-tap programmable FIR bandpass filter block diagram including time-interleaved sample-and-hold followed by four 32-tap FIR filters with controllable bandwidth.

Table 3.1: FIR filter coefficients to meet the desired filter bandwidths.

Coefficient	3 MHz	4 MHz	6 MHz	8 MHz	10 MHz	12 MHz	15 MHz	20 MHz	25 MHz	30 MHz
$\alpha_{0,32}$	0	0	0	0	0	0	0	0	0	0
$\alpha_{1,31}$	0.0081	0.0005	-0.0028	-0.0018	0.0002	0.0020	0.0026	-0.0010	-0.0026	0.0015
$\alpha_{2,30}$	-0.0012	-0.0002	0.0004	0.0004	0.0002	-0.0001	-0.0004	-0.0001	0.0004	0.0001
$\alpha_{3,29}$	-0.0157	-0.0040	0.0051	0.0061	0.0043	0.0008	-0.0043	-0.0049	0.0022	0.0056
$\alpha_{4,28}$	0.0067	0.0024	-0.0017	-0.0028	-0.0027	-0.0016	0.0007	0.0028	0.0010	-0.0025
$\alpha_{5,27}$	0.0263	0.0123	-0.0039	-0.0101	-0.0122	-0.0107	-0.0035	0.0095	0.0109	-0.0025
$\alpha_{6,26}$	-0.0186	-0.0107	0	0.0053	0.0084	0.0094	0.0070	-0.0023	-0.0089	-0.0058
$\alpha_{7,25}$	-0.0380	-0.0260	-0.0069	0.0046	0.0133	0.0192	0.0209	0.0083	-0.0103	-0.0213
$\alpha_{8,24}$	0.0387	0.0305	0.0150	0.0039	-0.0059	-0.0147	-0.0228	-0.0212	-0.0061	0.0161
$\alpha_{9,23}$	0.0464	0.0412	0.0283	0.0173	0.0061	-0.0057	-0.0208	-0.0331	-0.0283	-0.0052
$\alpha_{10,22}$	-0.0658	-0.0644	-0.0549	-0.0443	-0.0317	-0.0165	0.0069	0.0388	0.0544	0.0475
$\alpha_{11,21}$	-0.0465	-0.0493	-0.0490	-0.0457	-0.0405	-0.0330	-0.0191	0.0059	0.0276	0.0443
$\alpha_{12,20}$	0.0948	0.1070	0.1188	0.1214	0.1198	0.1140	0.0982	0.0601	0.0150	-0.0422
$\alpha_{13,19}$	0.0349	0.0414	0.0496	0.0538	0.0566	0.0584	0.0586	0.0542	0.0453	0.0290
$\alpha_{14,18}$	-0.1176	-0.1439	-0.1820	-0.2049	-0.2241	-0.2417	-0.2628	-0.2857	-0.2963	-0.2920
$\alpha_{15,17}$	-0.0130	-0.0163	-0.0212	-0.0244	-0.0272	-0.0301	-0.0341	-0.0399	-0.0451	-0.0505
α_{16}	0.1262	0.1586	0.2089	0.2417	0.2719	0.3027	0.3467	0.4152	0.4806	0.5578

In order to implement the desired FIR transfer function, first consider the circuit illustrated in Figure 3.3a which includes 32 transconductors, one capacitor, and switches controlled by the set of 34 non-overlapping clock phases shown in Figure 3.3b. The input voltage which is constant during an entire clock cycle is converted into a set of currents which, depending on the current clock phase, charge/discharge the capacitor. The total charge accumulated on the capacitor after 32 clock cycles and measured at the end of the process during clock phase ϕ_{34} is

$$Q_{C1}\left[\phi_{34}\right] = \sum_{i=1}^{32} g_{mi} v_{in}\left[\phi_i\right] T_{ck} \tag{3.3}$$

where T_{ck} is the period of the master clock clk. Since the charge is accumlated on a capacitor, the voltage at the evaluation phase is

$$V_O\left[\phi_{34}\right] = \frac{T_{ck}}{C} \sum_{i=1}^{32} g_{mi} v_{in}\left[\phi_i\right]. \tag{3.4}$$

Employing the z-transform of the discrete time equation leads to

$$\begin{aligned} V_O\left[z\right]\Big|_{\phi_{34}} &= \left(\frac{T_{ck}}{C}\right)\left(\sum_{i=1}^{32} g_{mi} z^{-i}\right) V_{in}\left[z\right] \\ &= \left(\frac{T_{ck}}{C} g_{m1} V_{in}\left[z\right]\right)\left(\sum_{i=1}^{32} \alpha_i z^{-i}\right) \end{aligned} \tag{3.5}$$

where the coefficient $\alpha_1 = 1$ and all other coefficients $\alpha_{2-32} = g_{m2-32}/g_{m1}$. It is clear that (3.5) resembles a typical discrete time filter transfer function thus enabling an FIR topology where the filter coefficients are implemented by ratios of transconductances making the overall filter shape less sensitive to PVT variations; the in-band gain, however is sensitive to PVT variations since g_{m1} itself will be susceptibe to PVT variations causing errors in the magnitude of the passband gain.

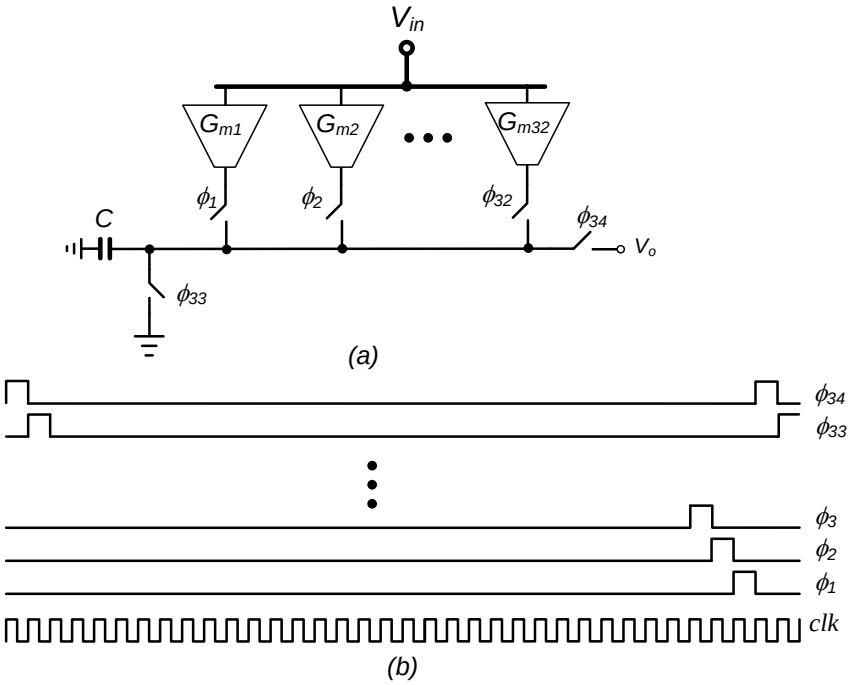


Figure 3.3: Single-tap implementation illustrating a) system level which includes 32 tunable transconductor cells, charge accumulation capacitor, and switches with b) 34 non-overlapping clock phases.

Although this architecture is interesting, filter latency is excessive; the overall sampling rate is only $T_{ck}/34$ which is too slow for the intended application. The circuit of Figure 3.3a can be expanded to the proposed FIR filter topology illustrated in Figure 3.4. This filter adds additional capacitors and a multiplexer (MUX) to allow the output signal to be taken from one capacitor each clock cycle. (3.5) can thus be extended to obtain the overall transfer function of

$$\frac{V_O[z]}{V_{in}[z]} = \left(\frac{g_{m1}T_{ck}}{C}\right)\left(\sum_{i=1}^{32}\alpha_i z^{-i}\right). \tag{3.6}$$

Figure 3.5 shows the magnitude response of the filter implemented with the co-

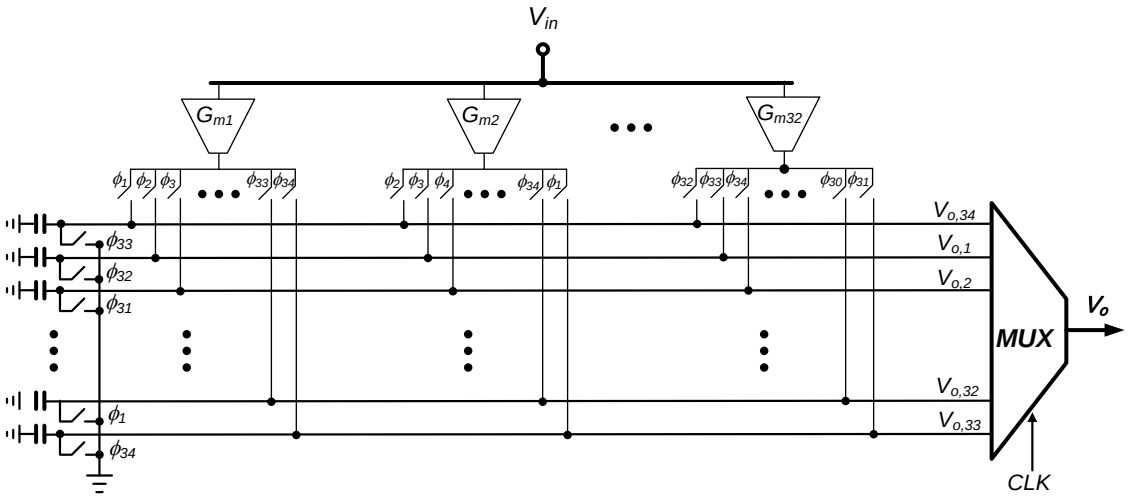


Figure 3.4: The 32-tap FIR filter architecture system level which includes 32 tunable transconductor cells, 34 capacitors, switches, and a multiplexer. The clock phases used are illustrated in Figure 3.3b.

efficients from Table 3.1. Bandwidths of 3, 10, and 30 MHz are shown. In Figure 3.6, the FIR filter coefficients are assumed to have a 20 percent random mismatch in the filter coefficients. Also illustrated are the ideal magnitude responses. As can be seen, the magnitude response is largely unaffected in the passband by mismatch in the filter coefficients. The main drawback is that the attenuation in the stopband is less well defined; however, the stopband attenuation is still large enough to meet the system specifications.

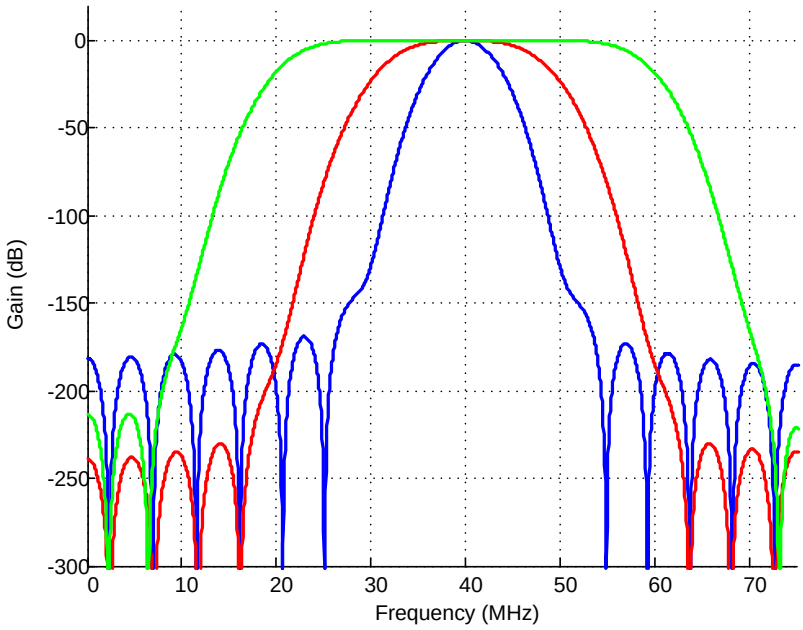


Figure 3.5: Magnitude response of FIR filter transfer functions for 3 (blue), 10 (red), and 30 (green) MHz bandwidths.

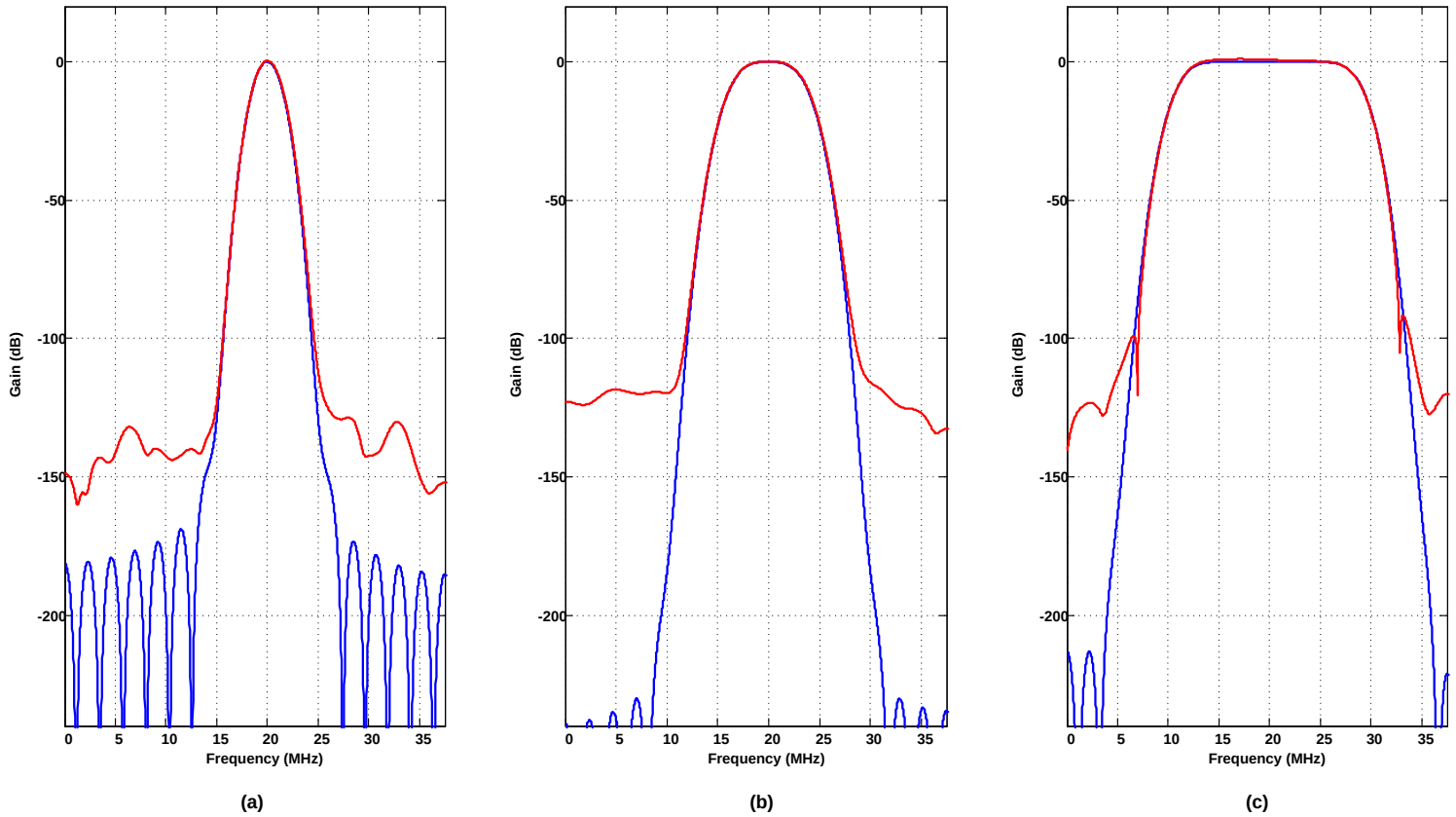


Figure 3.6: Magnitude responses of ideal filter (blue) and with 20 percent mismatch in filter coefficients (red). (a) 3 MHz bandwidth, (b) 10 MHz bandwidth, and (c) 30 MHz bandwidth.

3.2 Circuit Design

3.2.1 Sample-and-Hold

The input to the FIR filter needs to be constant during each clock period so that the charge injected onto the capacitor is proportionate to the sampled input voltage. Due to this, a typical sample-and-hold circuit which uses half the clock period to track the input signal cannot be used.

Figure 3.7 illustrates the proposed sample-and-hold circuit (single-ended representation shown for simplicity), which is a time-interleaved approach based on two flip-around sample-and-holds [48]. During one clock period, one of the two sample-and-hold circuits will track the input while the other holds a constant value. These operations will then switch for the following clock cycle, and so on. The sample-and-hold circuits each require two non-overlapping clock phases: one clock will turn the switches on to sample the input voltage onto the capacitor, while the second clock will be used to put the capacitor in feedback around the amplifier during the hold phase. These non-overlapping clock phases are generated by passing the 34 non-overlapping phases through two 17-input OR gates.

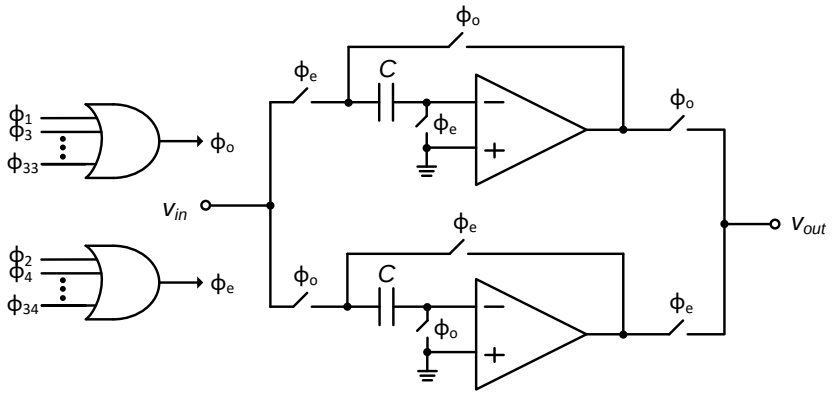


Figure 3.7: Time-interleaved sample-and-hold architecture.

Ideally, the output of the sample-and-hold would be constant during the entire hold phase which would allow the transconductor cells and capacitors that follow to do the desired integration error free; however, this is not the case due to the finite settling time of the amplifier. If a single pole amplifier is employed, the output of the sample-and-hold can be approximated to be

$$V_{O,SH}(t) = V_{O,ideal}\left(1 - e^{-t \times GBW}\right) \tag{3.7}$$

where GBW is the gain-bandwidth product of the amplifier's loop gain (including loading and feedback factor) and V_{O_ideal} is the output voltage after full settling. The sample-and-hold output drives the filter sections, and each FIR OTA output current is then integrated; thus, the final voltage increment on one of the capacitors of the filter of Figure 3.4 during one clock cycle is given by (3.8). In an ideal case with an infinite GBW, the voltage increment on the capacitor is (3.9).

$$\begin{aligned} V_C(t) &= \frac{1}{C}\int_0^{T_{ck}} g_{m,i} V_{O,SH}\left(1 - e^{-t \times GBW}\right) dt \\ &= \frac{1}{C} g_{m,i} V_{O,SH}\left(T_{ck} + \frac{e^{-T_{ck} \times GBW - 1}}{GBW}\right) \end{aligned} \tag{3.8}$$

$$V_{C,ideal} = \left(\frac{g_{m,i}}{C} T_{ck}\right) V_{O,SH} \tag{3.9}$$

Subtracting (3.8) from (3.9) gives the coefficient error which can be approximated as $1/(GBW \times T_{ck})$ with GBW in radians per second. For a sample rate of 150 MHz and an amplifier GBW of 600 MHz, the error accumulated in a clock period is less than four percent.

Following the sample-and-hold is the set of 32 transconductors for the FIR filter which has a total input capacitance of 3.8 pF. The amplifier topology used to meet the

GBW requirements while driving this large capacitive load is illustrated in Figure 3.8 which is a two-stage operational transconductance amplifier with a low power, high gain, folded-cascode configuration in the first stage and a high power feed-forward stage for amplifier stability [49]. There are two common-mode-feedback (CMFB) circuits used to stabilize the common-mode performance of the system and set the correct DC operating point. Figure 3.9 shows the schematic of the implementation of the amplifier with the bias generated by the circuit shown in Figure 3.10. A schematic of the amplifier's CMFB circuitry, originally introduced in [50], is illustrated in Figure 3.11. Table 3.2 lists the transistor sizes used in the amplifier with Table 3.3 listing the sizes of the transistors for the bias circuitry. The transistor sizes for the two CMFB circuits are given in Table 3.4.

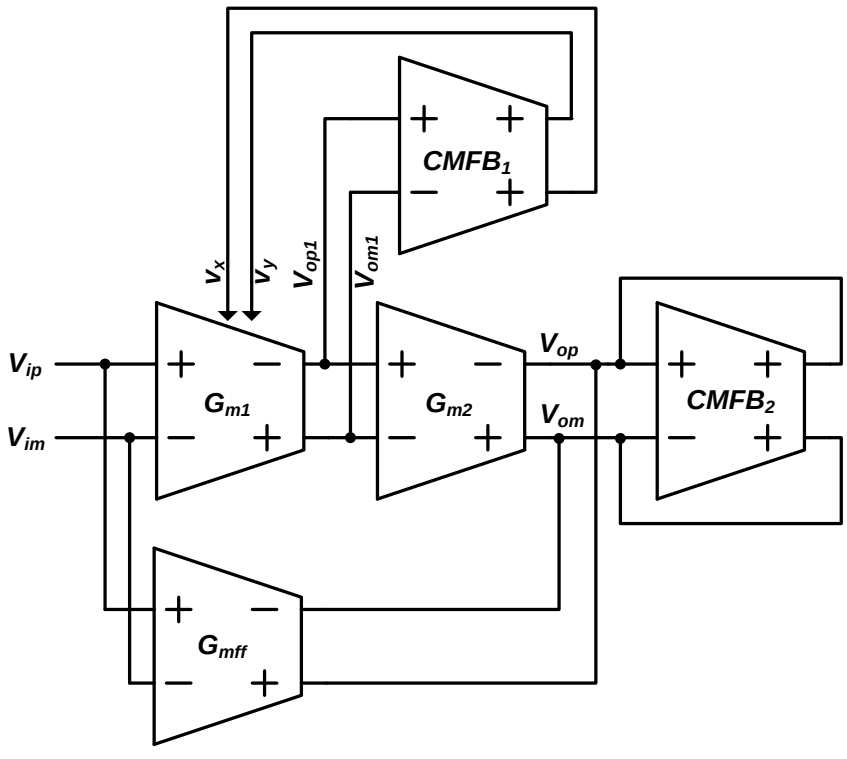


Figure 3.8: Sample-and-hold amplifier system level.

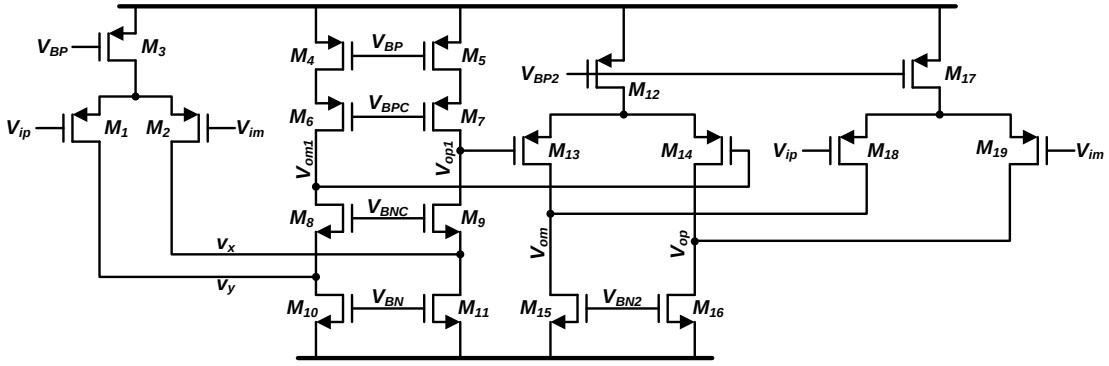


Figure 3.9: Sample-and-hold amplifier implementation.

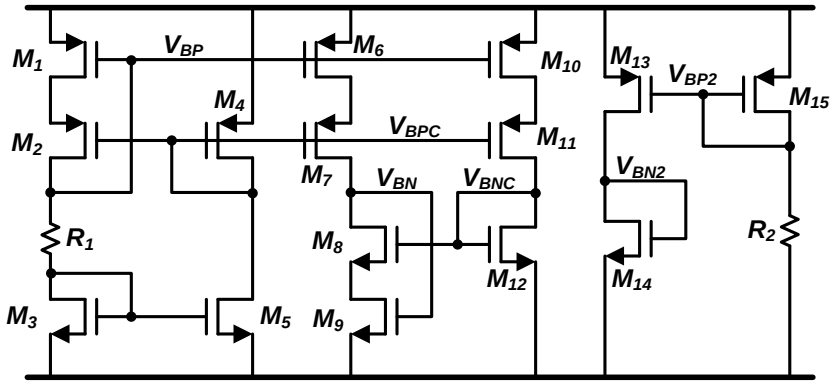


Figure 3.10: Sample-and-hold amplifier bias voltage generation.

Table 3.2: Transistor dimensions for OTA of Figure 3.9.

Transistor	Size (μm)
M_1, M_2, M_4, M_5, M_6, M_7	$\frac{40}{0.4}$
M_3	$\frac{80}{0.4}$
M_8, M_9	$\frac{10}{0.4}$
M_{10}, M_{11}	$\frac{20}{0.4}$
M_{12}, M_{13}, M_{14}, M_{17}, M_{18}, M_{19}	$\frac{260}{0.18}$
M_{15}, M_{16}	$\frac{100}{0.18}$

Table 3.3: Transistor dimensions for bias circuitry of Figure 3.10.

Transistor	Size (μm)
M_1, M_2, M_6, M_7, M_{10}, M_{11}	$\frac{40}{0.4}$
M_3, M_5, M_8, M_9	$\frac{10}{0.4}$
M_4	$\frac{16}{0.8}$
M_{12}	$\frac{8}{4}$
M_{13}, M_{15}	$\frac{60}{0.18}$
M_{14}	$\frac{40}{0.18}$
R_1	6 kΩ
R_2	800 Ω

Table 3.4: Transistor dimensions for CMFB circuitry of Figure 3.11.

Transistor	Size (μm) $CMFB_1$	Size (μm) $CMFB_2$
M_1	$\frac{160}{0.4}$	$\frac{240}{0.18}$
M_2, M_3, M_5, M_6	$\frac{20}{0.4}$	$\frac{30}{0.18}$
M_4	$\frac{80}{0.4}$	$\frac{120}{0.18}$
M_7, M_9	$\frac{10}{0.4}$	$\frac{60}{0.18}$
M_8	$\frac{20}{0.4}$	$\frac{120}{0.18}$

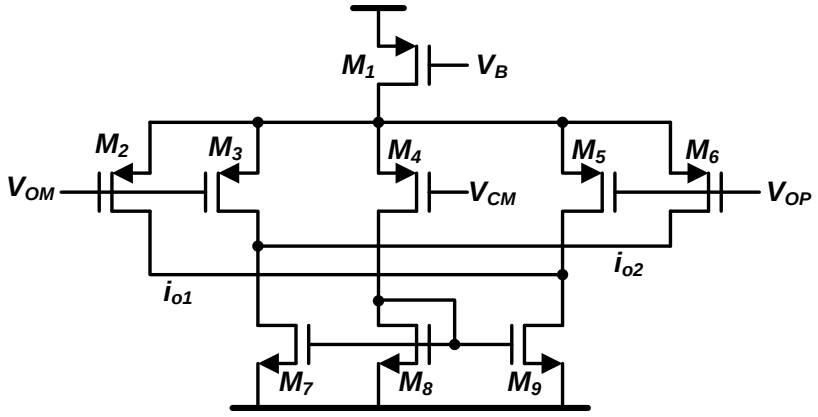


Figure 3.11: Sample-and-hold amplifier CMFB circuitry.

The amplifier was designed and simulated in Cadence with a 4 pF load which is approximately the input capacitance of the following set of transconductors. Figure 3.12 shows the magnitude and phase response of the amplifier when simulated in a typical process corner. The unity gain frequency is 660 MHz with 94° phase margin. The input referred noise spectral density is shown in Figure 3.13. The integrated output noise from 25 to 55 MHz is 2.12 μV^2 which gives an SNR or 43 dB for a 0 dBm input. This will not limit the performance of the system since the input SNR is likely to be negative.

The time-interleaved sample-and-hold was simulated in Cadence resulting in the transient response shown in Figure 3.14. As can be seen, due to the time-interleaved nature the sample-and-hold, the output is available for the full period of every clock cycle. With the large gain-bandwidth product in the amplifier, the system settles fast with no ringing due to sufficient available phase margin.

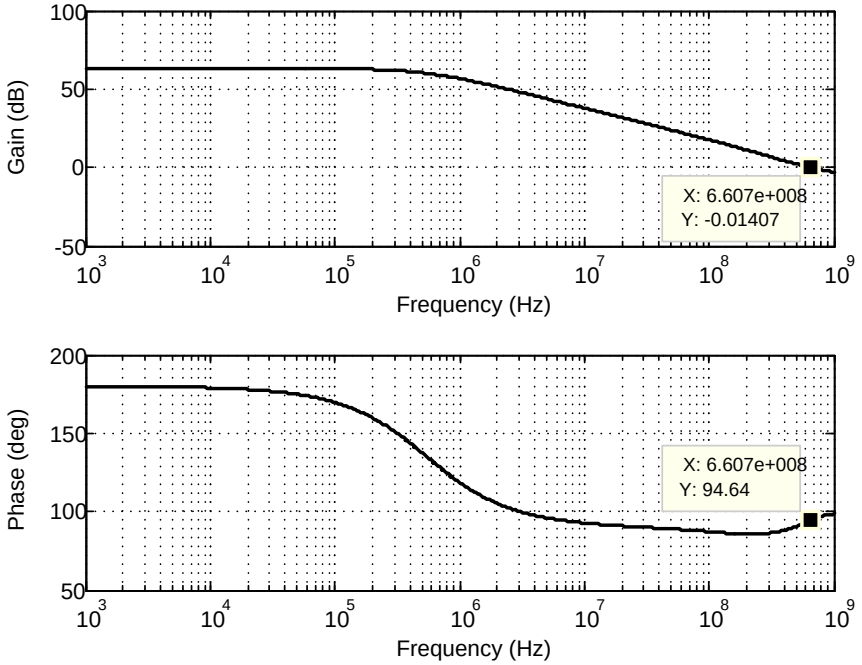


Figure 3.12: Sample-and-hold amplifier frequency response.

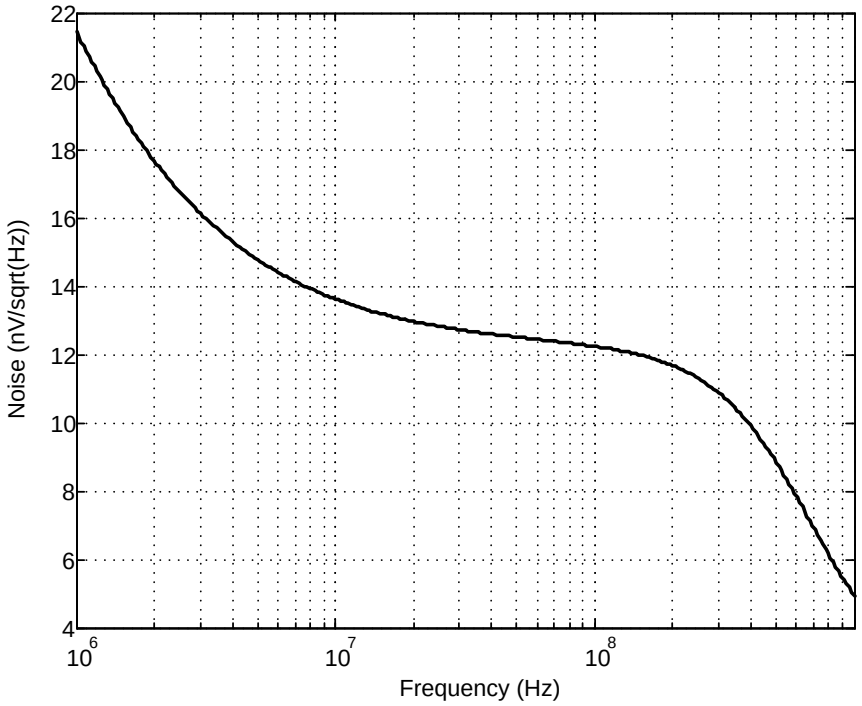


Figure 3.13: Sample-and-hold amplifier input referred noise spectral density.

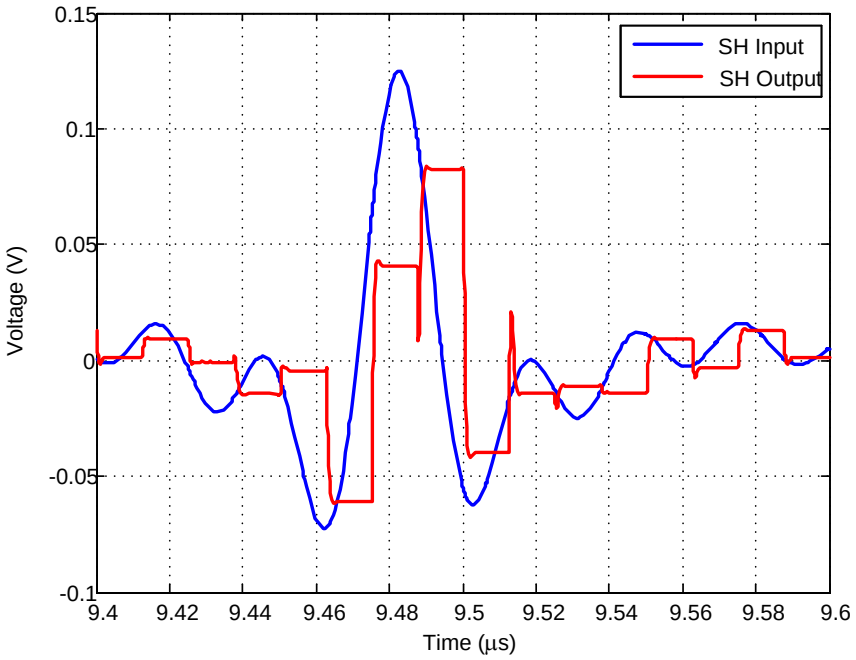


Figure 3.14: Sample-and-hold transient. Input signal shown in blue with sample-and-hold output in red.

3.2.2 Tunable Transconductor Cell

One of the main challenges in the design of this filter topology is the design of the transconductors cells. Since the capacitors of Figure 3.4 are fixed, the transconductors must be tunable in both magnitude and polarity in order to implement the required filter coefficients given in Table 3.1. With the capacitors set to 1 pF and a sampling rate of 150 MHz, using (3.5), the transconductances are derived and listed in Table 3.5. Ranging in transconductances from approximately 95 μA/V to less than 1 μA/V, each transconductor cell must be tunable in both magnitude and polarity across a broad range of values that do not follow any sort of common pattern between filter bandwidth selections. For each filter bandwidth setting, there are only 16 transconductance values needed since the filter is symmetric. In all cases, if the required transconductance was less than 0.1 μA/V in magnitude it was set to zero. MATLAB simulations show that doing this has minimal affect on the filter's passband as can be seen in Figure 3.15 – only the stopband attenuation decreases from approximately -250 dB to -100 dB when the smallest transconductors are set to zero and a 20 percent random mismatch in the remaining filter coefficients is included.

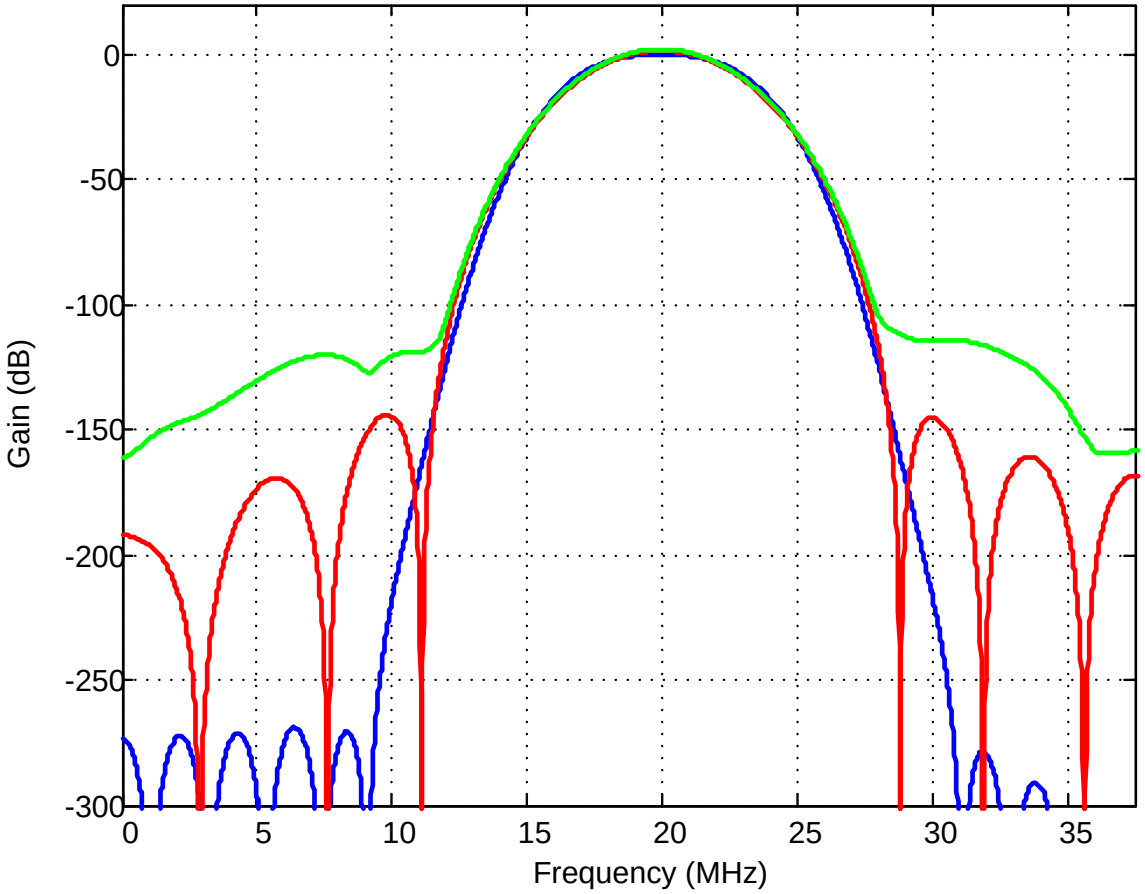


Figure 3.15: MATLAB plot illustrating the filter tolerance to setting the smallest transconductances to 0. The 8 MHz bandwidth case is plotted. The blue waveform is the ideal transfer function. The red waveform shows the magnitude response when g_m cells less than 0.1 μA/V are set to 0. The green waveform includes 20 percent random mismatch in the coefficients.

Table 3.5: Transconductance values needed to implement FIR filter coefficients for the desired filter bandwidths. Listed G_m values are in μA/V.

Coefficient	3 MHz	4 MHz	6 MHz	8 MHz	10 MHz	12 MHz	15 MHz	20 MHz	25 MHz	30 MHz
$\alpha_{0,32}$	0	0	0	0	0	0	0	0	0	0
$\alpha_{1,31}$	0	0	0	0	0	0.3	0.4	0.2	0.4	0.2
$\alpha_{2,30}$	0	0	0	0	0	0	-0.1	0	-0.1	0
$\alpha_{3,29}$	-2.7	0	0	0	0.7	0.1	-0.7	0.8	-0.4	1.0
$\alpha_{4,28}$	0	0	0	0	-0.5	-0.3	0.1	-0.5	-0.2	-0.4
$\alpha_{5,27}$	4.5	2.1	0	0	-2.1	-1.8	-0.6	-1.6	-1.9	-0.4
$\alpha_{6,26}$	-3.2	-1.8	0	0	1.4	1.6	1.2	0.4	1.5	-1.0
$\alpha_{7,25}$	-6.5	-4.4	0	0	2.3	3.3	3.6	-1.4	1.7	-3.6
$\alpha_{8,24}$	6.6	5.2	-2.5	0	-1.0	-2.5	-3.9	3.6	1.0	2.7
$\alpha_{9,23}$	7.9	7.1	-4.8	-3.0	1.0	-1.0	-3.5	5.6	4.8	-0.9
$\alpha_{10,22}$	-11.2	-11.0	9.4	7.6	-5.4	-2.8	1.2	-6.6	-9.3	8.1
$\alpha_{11,21}$	-7.9	-8.4	8.3	7.8	-6.9	-5.6	-3.3	-1.0	-4.7	7.5
$\alpha_{12,20}$	16.2	18.3	-20.2	-20.8	20.5	19.4	16.7	-10.2	-2.6	-7.2
$\alpha_{13,19}$	6.0	7.1	-8.5	-9.2	9.7	9.9	10.0	-9.2	-7.7	4.9
$\alpha_{14,18}$	-20.1	-24.6	31.0	25.0	-38.3	-41.1	-44.8	48.5	50.5	-49.7
$\alpha_{15,17}$	-2.2	-2.8	3.6	4.2	-4.7	-5.1	-5.8	6.8	7.7	-8.6
α_{16}	21.5	27.1	-35.6	-41.3	46.5	51.4	59.1	-70.5	-81.9	94.9

Since the required transconductance values vary by several orders of magnitude, it would be very difficult and inefficient to design a single device that can meet every requirement. In this design, five different transconductors were designed with the following transconductance tuning ranges: 0.2 to 2 μA/V, 0.7 to 6 μA/V, 1 to 11 μA/V, 4 to 20 μA/V, and 20 to 90 μA/V.

The schematic of the proposed widely tunable transconductor design is shown in Figure 3.16a. The transconductor consists of a basic source degenerated differential pair with a current mirror load. The transistors M_{T1}–M_{T6} are placed across the drain of the transistors in the differential pair and, along with the replica circuit shown in Figure 3.16b, are used to tune the transconductance by attenuating the differential current entering into the current mirror load. The tuning transistors M_{T1}–M_{T6} operate in the triode region when activated and present a resistance of R_{tune} that is controlled by the gate voltage set to $2V_{GS2}$. Due to the current division which is illustrated in Figure 3.17, the total low frequency current being mirrored from M_2 to M_3 is then computed as

$$i_{out} = V_{in} \times \frac{g_{m1}}{1 + g_{m1}R_S} \times \frac{\frac{R_{tune}}{2}}{\frac{R_{tune}}{2} + \frac{1}{g_{m2}}}. \tag{3.10}$$

Due to the replica circuit of Figure 3.16b, the overdrive voltage $V_{GS} - V_T$ of M_2 and M_T is similar which gives an overall low frequency transconductance that can be approximated as

$$G_m = \frac{g_{m1}}{1 + g_{m1}R_S} \times \frac{1}{1 + 2 \times \frac{(W/L)_T}{(W/L)_2}}. \tag{3.11}$$

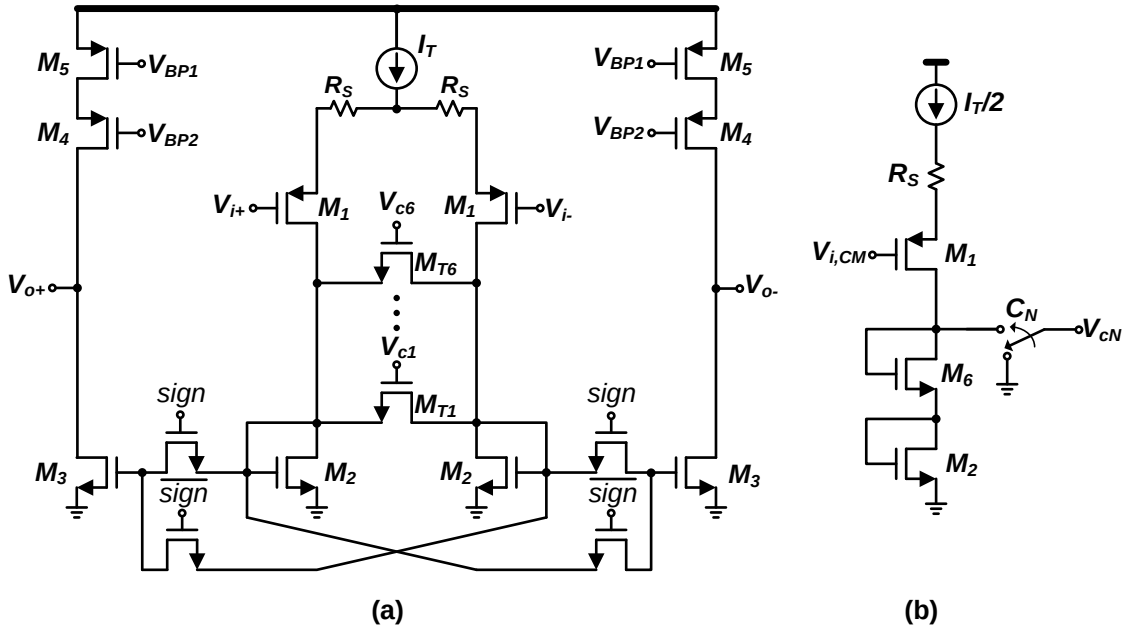


Figure 3.16: (a) Tunable transconductance topology with polarity control and (b) replica circuit for tuning voltage reference generation.

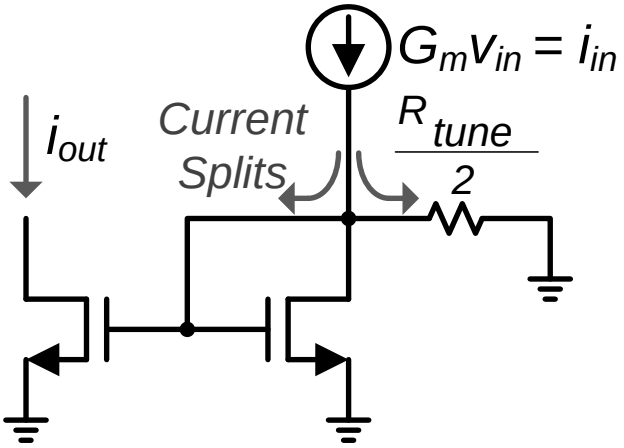


Figure 3.17: How the current splits in the tunable transconductors.

The transconductance can thus be tuned by adjusting the ratio of two transistor dimensions which is reliable with PVT variations. The tuning is carried out through a bank of transistors, $M_{T1} - M_{T6}$, which allows the adjustment of $(W/L)_T$ without affecting the OTA's operating point. However, g_m itself is susceptible to PVT variations which can give a gain error in the FIR filter according to (3.5). A tuning scheme can be used if better accuracy is needed in the FIR filter gain but was not included in the reported design because accurate passband gain was not a critical design parameter for the radar matched filter application which mainly serves the purpose of maintaining the envelope shape of the received pulse signal.

The input referred thermal noise of the transconductor cells is a function of the OTA transconductance values and can be calculated to be

$$\begin{aligned} v_{n,in}^2 = 8kT \left(\frac{1 + g_{m1} R_S}{g_{m1}} \right)^2 \Bigg[& \frac{\gamma}{A_{cd}^2} \left(g_{m3} + g_{m5} \right) + \gamma g_{m2} \\ & + \frac{2}{r_{ds,T}} + \left(R_S g_{m1}^2 + \gamma g_{m1} \right) \left(\frac{1}{1 + g_{m1} R_S} \right)^2 \Bigg] \end{aligned} \tag{3.12}$$

where γ is the noise fitting factor and is typically between 2/3 and 1; meanwhile, the A_{cd} factor represents the current division gain between the diode connected transistor M_2 and the tuning transistor M_T and is calculated to be

$$A_{cd} = \frac{g_{m2} r_{ds,T}}{2 + g_{m2} r_{ds,T}}. \tag{3.13}$$

This results in a noise power density ranging from -149 dBm/Hz$^{1/2}$ when all of the tuning switches are off (maximum transconductance gain) to -121 dBm/Hz$^{1/2}$ when they are all switched on (minimum transconductance gain), which is the worst case since the current division factor is maximum under these conditions. According to Table 3.5, the two most dominant transconductors of Figure 3.4, g_{m14} and g_{m16},

will both have their highest noise level when the filter bandwidth is at its minimum; therefore, total integrated noise will stay fairly constant across all bandwidth selections; this result agrees with the fact that noise is usually dominated by kT/C, and in this filter realization the load capacitor remains constant.

Table 3.6 lists the sizes of the transistors and resistors for the transconductor cells. Achievable transconductance values for the 20 to 90 μA/V transconductor cell are shown in Figure 3.18. Five control bits were used to achieve the required values needed to generate the FIR filter coefficients. An additional sixth control bit was used to provide polarity control to switch the transconductor's gain between positive and negative values. Table 3.7 summarizes the performance metrics of the 20 to 90 μA/V transconductors. The remaining four tunable transconductor cells have similar performance.

Table 3.6: Device sizes for the 20 – 90 μA/V transconductance cell. All transistor sizes are in μm.

Component	Size
M_1	16/1
M_2	3/1
M_3	3/1
M_4	10/0.4
M_5	10/0.4
M_6	3/1
M_T	0.22/0.8 to 3.52/0.8
R_S	4 kΩ
C_S	650 fF

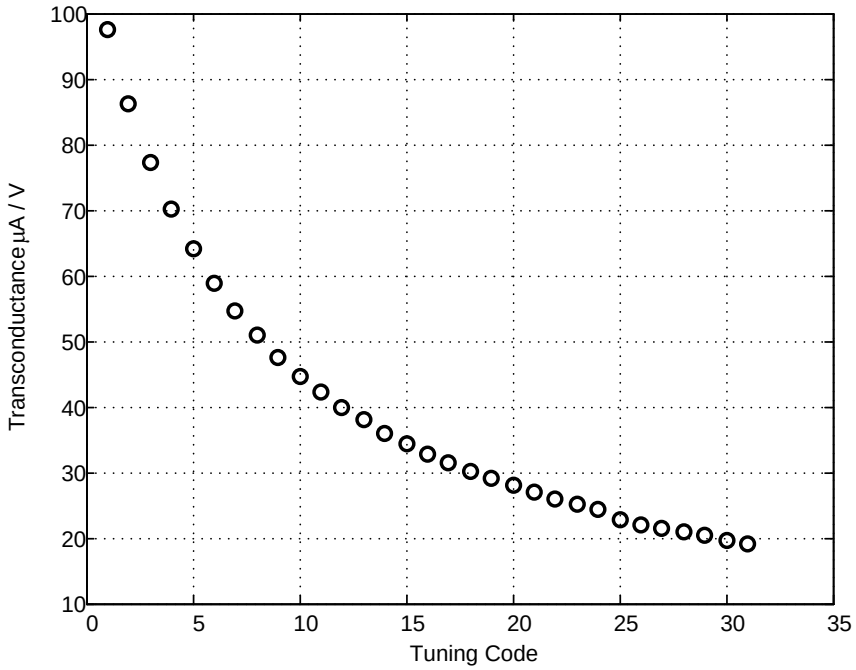


Figure 3.18: Tunability of 20–90 μA/V transconductor. Five control bits were used to access values across the desired range.

3.2.3 Active Multiplexer

The simplified single-ended schematic of the multiplexer is illustrated in Figure 3.19 which is a time-interleaved topology similar to the one used in the sample-and-hold. During the even numbered clock phases, the charge from the desired capacitor is injected onto the capacitor C_{fb} that, in conjunction with the amplifier, holds the output voltage until the next cycle; meanwhile in the second amplifier, the voltage across the feedback capacitor is being reset to zero to prepare it for its upcoming hold phase.

Table 3.7: Performance metrics of the 20–90 μA/V transconductance cell.

Component	Size
G_m Range	20–90 μA/V
IIP3	>16 dBm
Power Noise Density	< -132 dBm/Hz$^{1/2}$
Power Consumption	316 μW

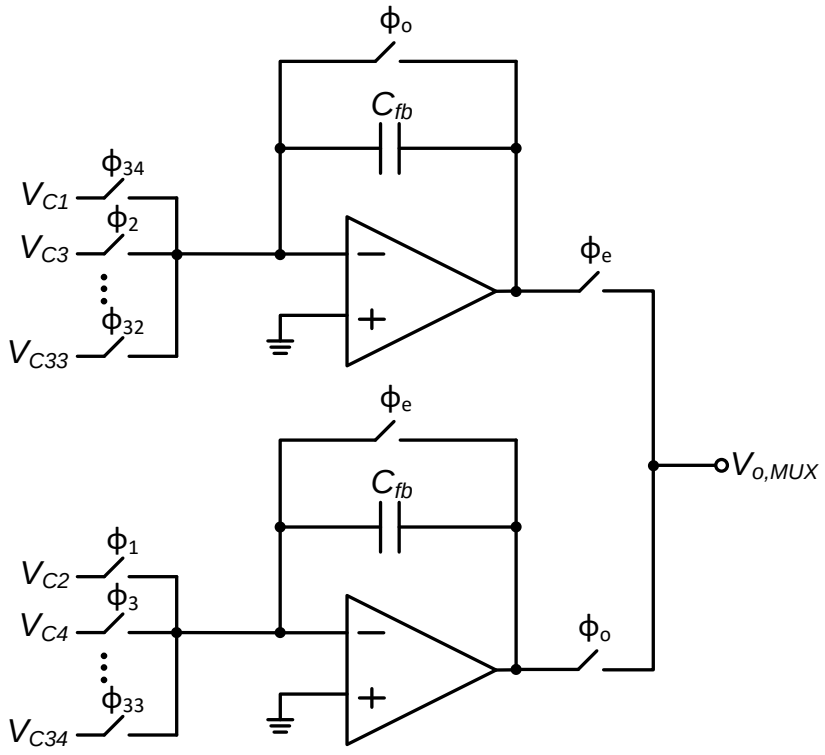


Figure 3.19: Time-interleaved MUX topology.

The amplifier needs to drive the following stage which consists of the set of tunable transconductors in the same manner that the sample-and-hold must drive the first stage's transconductors. This makes the requirements for the amplifier of the multiplexer to be the same as that of the sample-and-hold, so the same amplifier topology is used here. The GBW of the amplifier is greater than 600 MHz when driving a 3.8 pF load capacitance (input capacitance of following transconductors) with each amplifier consuming 47 mW.

3.2.4 34-Phase Non-Overlapping Clock Generator

Of key importance in the operation of the FIR filter is the generation of the 34 non-overlapping clock phases. For the proposed solution, a differential ring oscillator is locked with the reference clock to synchronously oscillate at a frequency equal to 150/34 MHz as illustrated in Figure 3.20 [51]. At the input there is a divide by 2 which produces a 75 MHz output which drives the ring oscillator. The ring oscillator then provides an addition division by 17. There is a second ring oscillator doing the same operation with the input being the inversion of the 75 MHz reference clock. The auxillary inverters lock the two ring oscillators such that their transitions are all synchronized. The 34 outputs will thus be 75/17 MHz clocks with equal delay spacing across the entire clock period. The injection locking technique dictates when the transitions of the ring oscillator will happen; thus the jitter performance of the ring oscillator output is correlated with that of the master clock.

The non-overlapping behavior is obtained by adding delay elements at ClkB output of each inverter stage as shown in Figure 3.21. These delayed and inverted clocks allow the required non-overlapping clock signals to be obtained. For example, clock phase ϕ_1 is obtained by ANDing the clock phases Ck1B and Ck2 as depicted in Figure 3.22. Similarly, clock phase ϕ_2 is obtained by ANDing Ck2B and Ck3. The

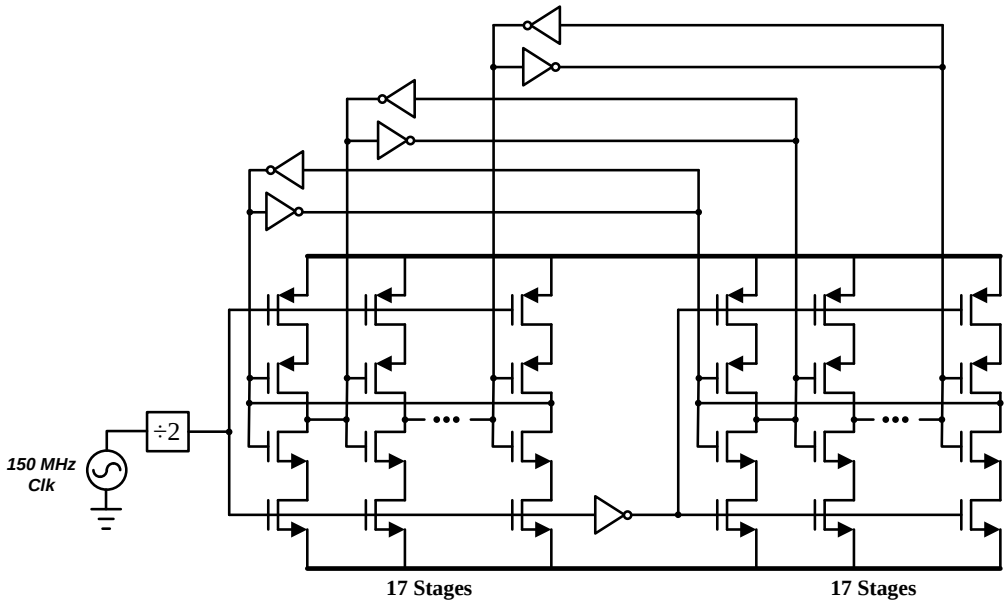


Figure 3.20: 17-stage injection locked ring oscillator used for the generation of the 34 non-overlapping clock phases.

non-overlapping time is defined by the delay of the digital buffers used.

The clock generator was design and simulated in Cadence. Figure 3.23 shows the transient responses of the input reference clock and one of the ring oscillator outputs. The ring oscillator divides the frequency by 17 as expected. The 34 non-overlapping clock phases are illustrated in Figure 3.24. It is difficult to see any transitions in this figure, so Figure 3.25 is added which shows the non-overlapping behavior of a few phases.

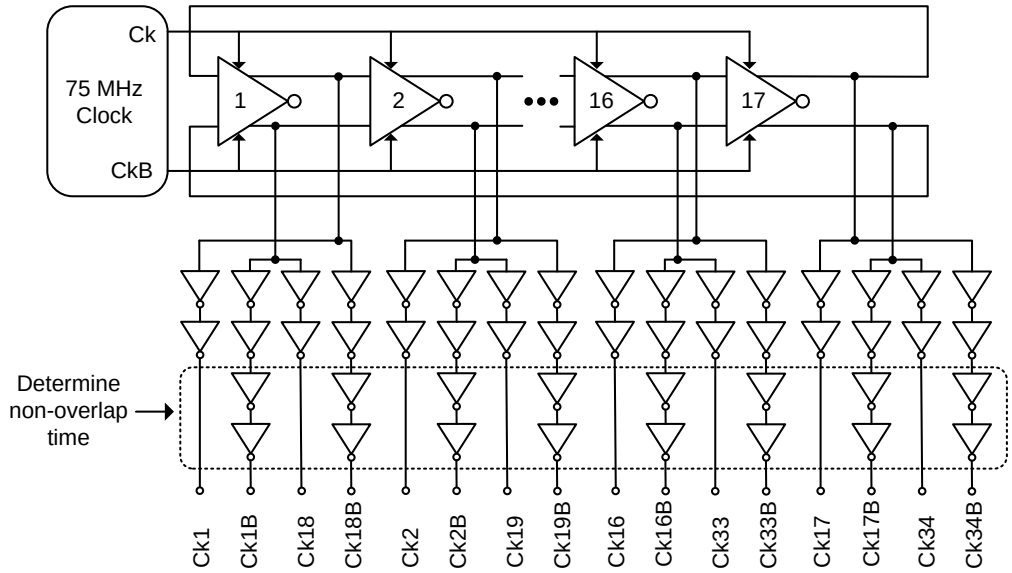


Figure 3.21: Clock signals used in the generation of the 34 non-overlapping clock phases.

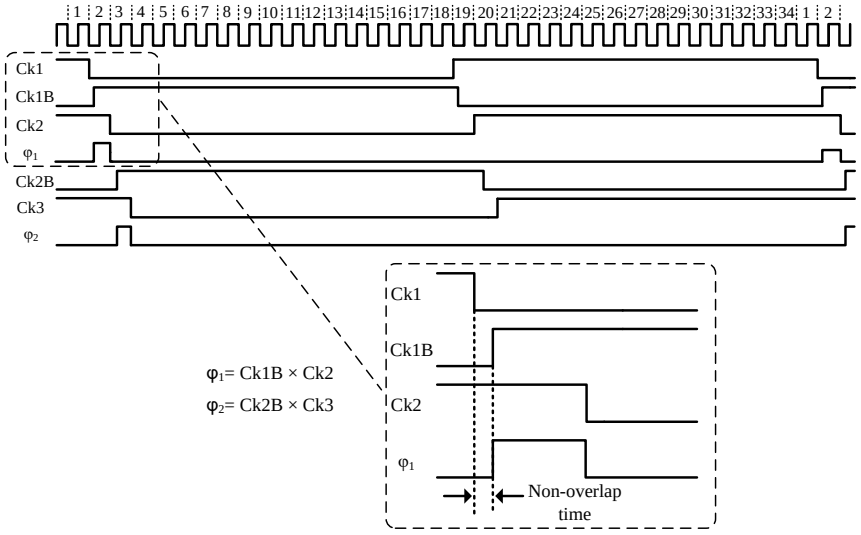


Figure 3.22: Generation of the non-overlapping clock phases.

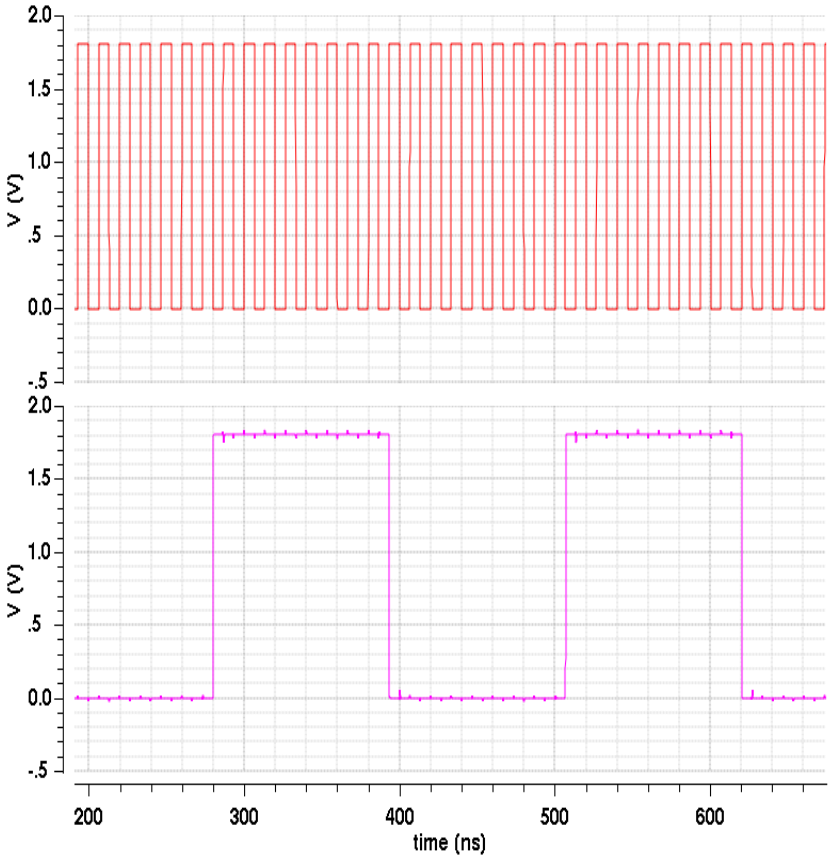


Figure 3.23: Input and output of ring oscillator.

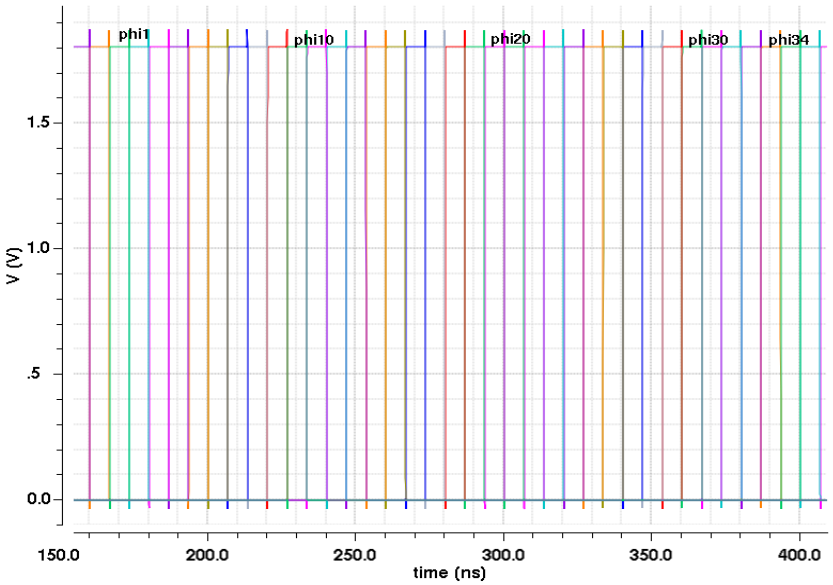


Figure 3.24: 34 non-overlapping clock phase generator output.

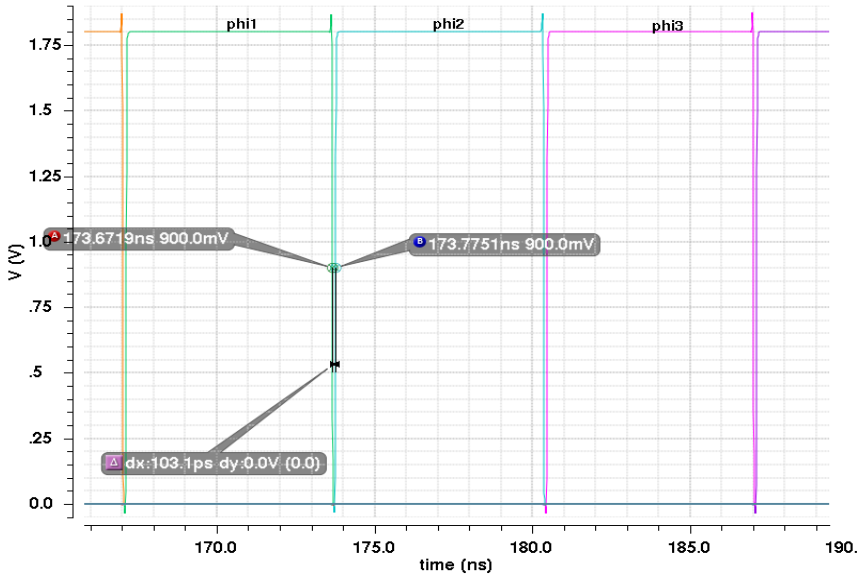


Figure 3.25: Simulation of clock generator showing non-overlapping time.

3.2.5 Switch Design

All switches used are single NMOS transistors. The common-mode voltage throughout the sytem was set to 600 mV instead of the typical choice of $V_{DD}/2 = 900$ mV. With a 1.8 V supply, this allows sufficient overdrive voltage on the switches remedying the need for a full transmission gate. The switches used are 1.0 μm/0.18 μm which produces the switch resistance curve shown in Figure 3.26. For small signals located around 600 mV, the switch resistance is approximately 1 kΩ. For larger signals of around 250 mV amplitude, the switch resistance nears 2 kΩ. Since the OTA output is current, the maximum voltage drop across the switches will be about 45 mV which is small enough to keep the switches in the correct operating region. The small switch size minimizes the effect of clock feedthrough and charge injection issues.

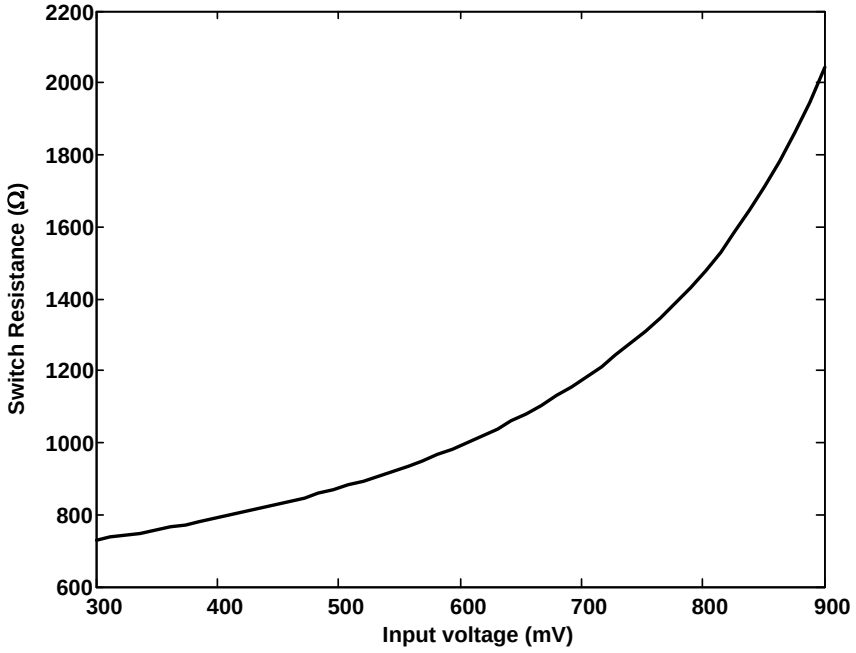


Figure 3.26: Switch resistance curve vs. input voltage.

3.3 Measurement Results

The filter was fabricated in a Jazz 0.18 μm SOI process [18] and designed to have an IF frequency of 40 MHz with a bandwidth tunable from 3 MHz to 30 MHz. Figure 3.27 shows the die microphotograph of the fabricated filter. The full chip area is 2×3 mm^2 with the main filter area being approximately 1.6×2.1 mm^2. The four filter stages consume the majority of the area. The non-overlapping clock generation is centrally located to minimize delay differences in the individual phases as they are distributed to the switches in the filter stages.

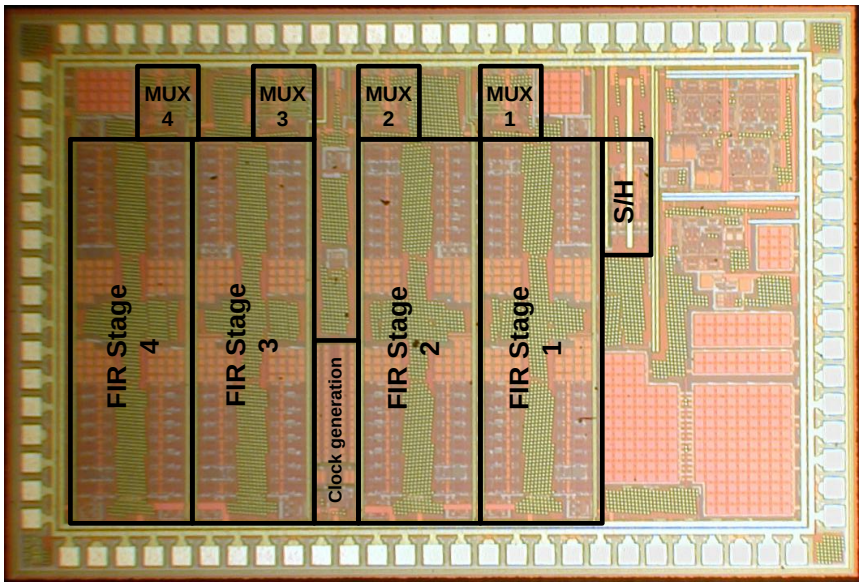
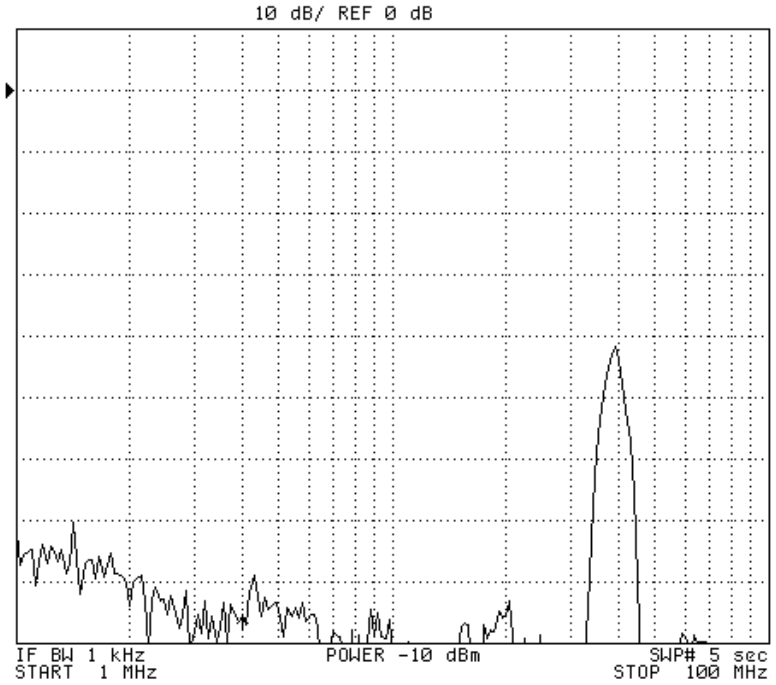


Figure 3.27: Microphotograph of the 2mm $\times$ 3mm FIR filter chip with 1.6mm $\times$ 2.1mm active area.

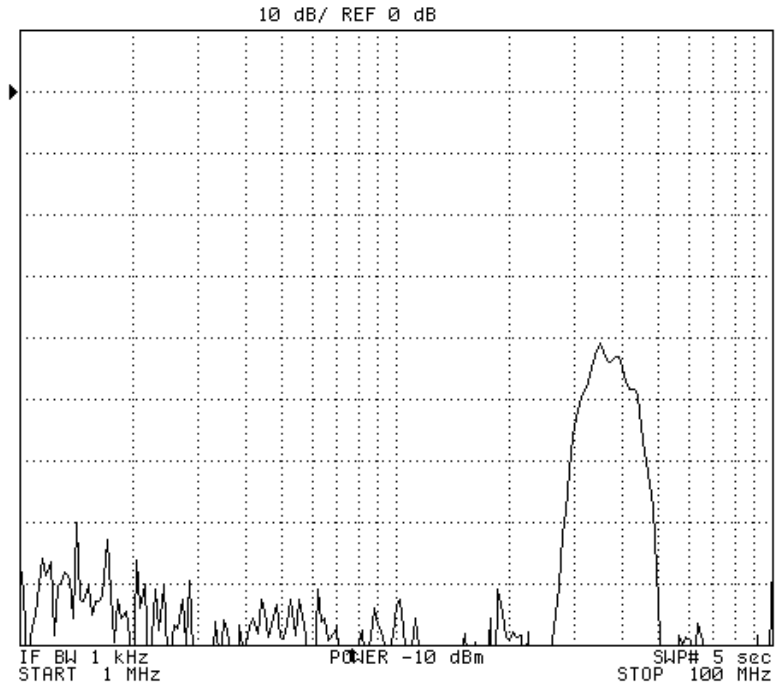
The filter consumes approximately 300 mA from a 1.8 V supply for a total power consumption of 540 mW. Each tunable OTA consumes approximately 195 μW. The core filter power, i.e. the power not including the sample-and-hold, is 450 mW. The

majority of the power consumption is from the amplifiers used in the MUX which each consume 47 mW due to their need to drive a 3.8 pF load while maintaining fast settling time performance. In this design, the final FIR stage had to drive the pads and active probes which have comparable input impedance to the transconductors; however, in the radar system, a 1-bit ADC follows the FIR filter so the load capacitance will be greatly reduced to less than 100 fF [3, 52]. The final stage amplifier could therefore be scaled down to use less than 1 mW each representing a savings of 92 mW, or about a 20 percent reduction in total filter power.

To measure the frequency response of the FIR filter, a network analyzer was used. Figure 3.28 shows the magnitude response of the filter with bandwidth selections of 3 MHz and 8 MHz. As can be seen there is a large attenuation in the magnitude response, even at the center frequency. When the filter was being designed, the pull-down switch of Figure 3.16b was unfortunately omitted leaving the gates of the tuning transitors floating when they should have been pulled down to ground. This missing switch is illustrated in Figure 3.29. This caused a large attenuation and passband rolloff that will be seen in the following measurement results. In order to get improved measurement results, in the lab the sample rate was decreased from 150 MHz to 75 MHz which has the effects of boosting the gain according to (3.6), reducing the IF frequency from 40 MHz to 20 MHz, and cutting all bandwidths in half. The attenuation should reach the desired 40 dB by 5 MHz now instead of 10 MHz.



(a)



(b)

Figure 3.28: Measured magnitude response of FIR filter at 40 MHz IF. (a) 3 MHz bandwidth and (b) 8 MHz bandwidth.

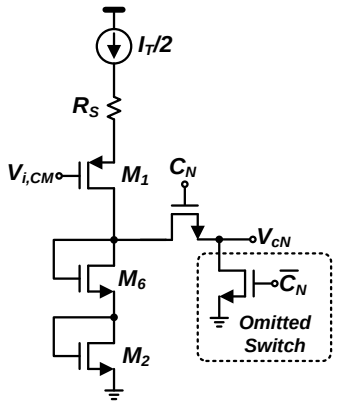


Figure 3.29: Pull down switch that is missing leaving tuning transistor gates floating when they should be pulled to ground.

The magnitude response of the FIR filter is illustrated in Figure 3.30a; bandwidth selections of 1.5, 7.5, and 15 MHz are shown. The center frequency is near 20 MHz, and there is a sharp near rectangular roll-off in the transition from the passband to stopband to help suppress all of the received radar pulse's thermal noise and blockers that are not in the passband of the filter. Nearly 50 dB attenuation is achieved in the stopband. The droop in gain evident in the wider bandwidth cases is due to the floating gates of the tuning transistors. This effect is most prevalent during the wider bandwidth cases. The rolloff in the stopband is appoximately a $sinc^4(f)$ shape. This effect can be removed in the digital domain by additional signal processing. Figure 3.30b shows the case when the waveforms are compensated in MATLAB.

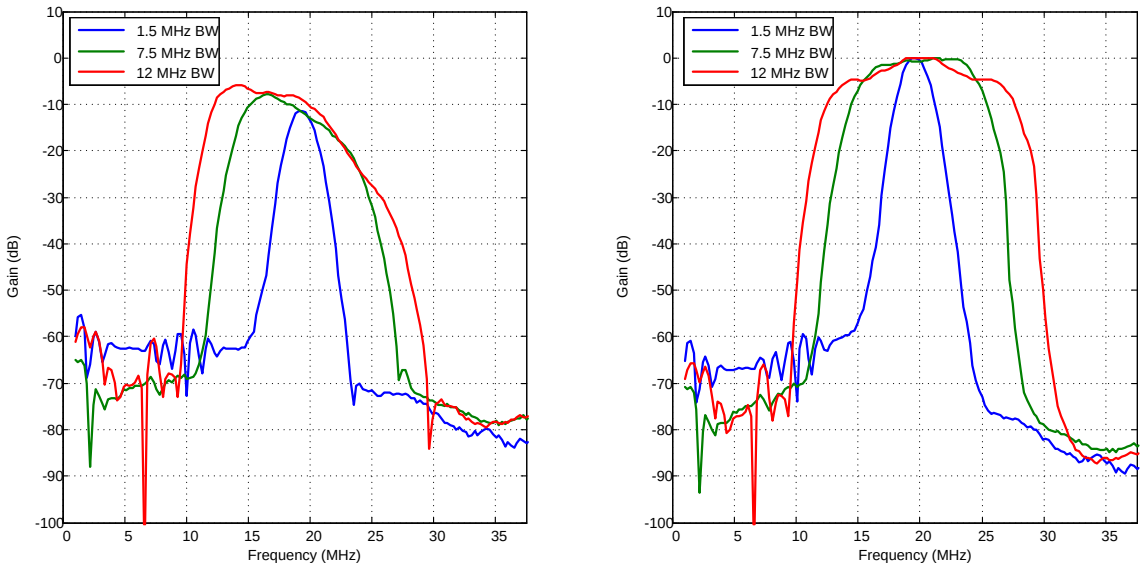


Figure 3.30: (a) Measured magnitude response of FIR filter. Bandwidths of 1.5, 7.5, and 15 MHz are shown. (b) Measured magnitude response after being compensated for the *sinc* distortion that appears in (a) due to the missing pull-down switch in the tuning transistors.

For testing the linearity of the highly selective bandpass filter, a two-tone test

was done with input frequency tones of 19.9 and 20.1 MHz. Figure 3.31 shows a plot of the IIP3 for each bandwidth selection. The worst case IIP3 of 8.5 dBm occurs when the filter is set to 12.5 MHz bandwidth. In this case, as shown in Table 3.5, none of the transconductors are set to zero, therefore the most non-linearities are being introduced. When the system has the most transconductors zeroed, i.e. the 4 MHz bandwidth, the linearity reaches its maximum of approximately 11.7 dBm.

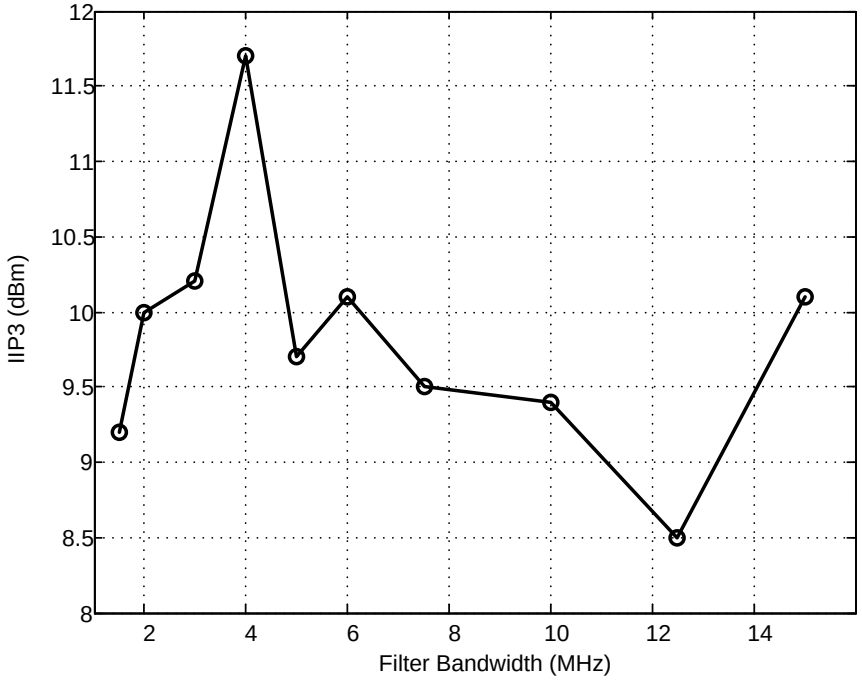


Figure 3.31: Measured IIP3 across all filter bandwidths.

To measure the noise performance of the filter, a 50 Ω load was attached to the input of the filter. The noise spectrum at the filter output plus buffers was measured for each bandwidth. The output noise spectral density was integrated to find the total noise that appears at the output as shown in Figure 3.32. These values fit well with the estimated noise level discussed in Section 3.2.2.

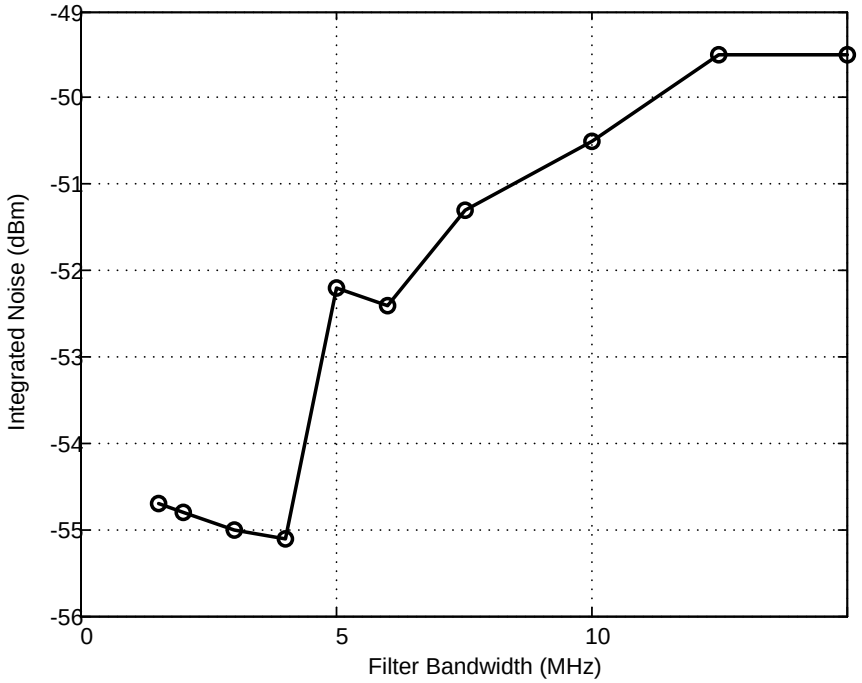


Figure 3.32: Total integrated ouput noise power for each bandwidth selection.

One of the main requirements of this filter was to have a linear phase response so that the pulsed waveform could pass through the filter without large amounts of dispersion in the time domain. Due to the sampling operation at the input of the filter, it is difficult to get meaningful group delay information from a network analyzer because network analyzers often measure delay by looking at the zero crossings. By varying the initial input phase, the sample-and-hold delay can vary by the sample period which is illustrated in Figure 3.33. Because of this constraint, pulses of varying frequency across the filter's passband were input into the filter and the output was measured. The envelope of the input and outputs were obtained and used to calculate the overall delay. Figure 3.34 shows the pulse delay averaged across the bandwidth of each filter bandwidth selection. Also shown is the standard deviation. Included in these results is also the variation introduced by the sample-and-hold circuitry

which is in the range of $\pm T_S/2 = 6.67$ ns; the true variation in group delay in each bandwidth selection of the filter itself will be less than what is shown. To minimize this issue, it is recommended to increase the oversampling ratio (e.g. > 5) that evidently results in a trade-off since power increases. Also, when increasing the sample rate, it becomes more difficult to achieve small bandwidths without further increasing the filter order which again would result in a power increase.

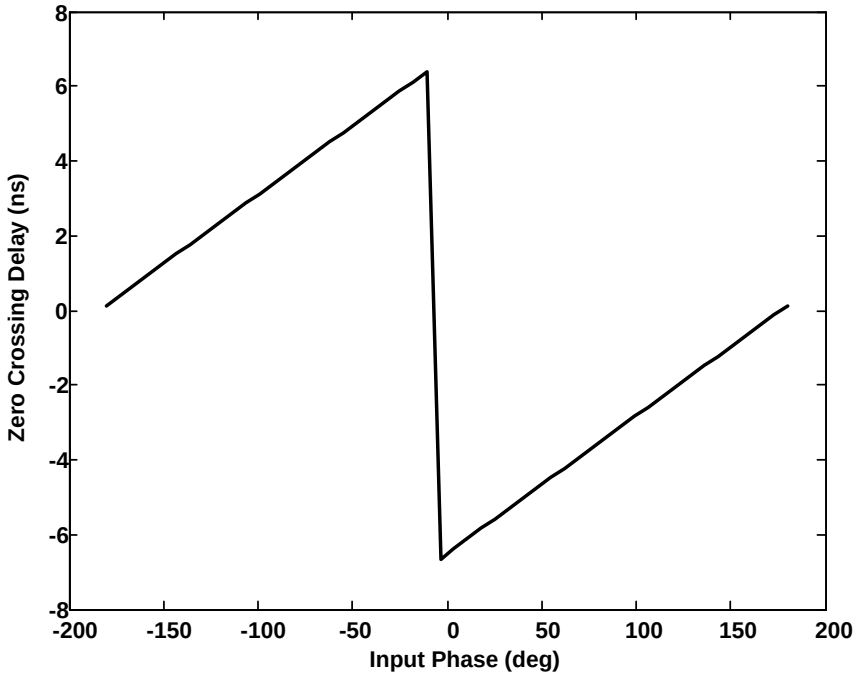


Figure 3.33: Zero crossing based delay detection varies when initial phase is changed.

Table 3.8 summarizes the performance and compares with previously published results. Reference [23] presented a bandpass filter centered at 57 MHz with a fixed bandwidth. By varying the sample rate, its center frequency shifted; however its bandwidth stayed fairly constant in the 1 to 2 MHz range. Reference [39] implemented a lowpass filter with a tunable bandwidth that could potentially be used

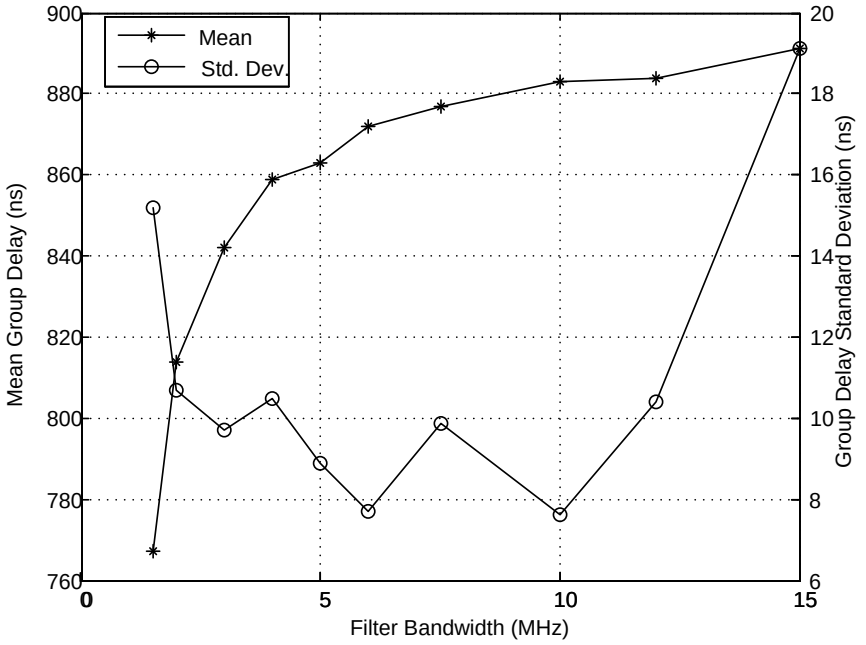


Figure 3.34: Mean pulse delay averaged over the filter bandwidth with the standard deviation illustrated as well. These results include the variations introduced due to the SH.

in a direct conversion radar receiver but exhibits a much lower IIP3. To the best of the author's knowledge, the filter presented in this dissertation presents the only widely tunable bandwidth bandpass FIR filter. While using more power than other approaches, this drawback is not a concern for a radar system that has power amplifiers operating at greater than 10 W. This new architecture allows complete control over the filter's transfer function at the expense of having one transconductor per coefficient. The attenuation at 5 MHz from the corner frequency was extrapolated from the magnitude response plots published in the papers. Although fabricated in a 0.18 μm technology, the proposed solution consumes only 3.5 mW per tap. This solution offers unmatched attenuation factors in the stopband.

Table 3.8: Summary and comparison of previous publications.

Ref	Technology	Bandwidth (MHz)	Attenuation at 5 MHz from BW (dB)	IIP3 (dBm)	Number of Taps	Power per Tap (mW)	Power (mW)
[23]	350 nm CMOS	2	$<$ -10	NR	15	9	136
[39]	65 nm CMOS	5–26	$<$ -30	-19	12	0.7	8.4
This Work	180 nm SOI CMOS	1.5–15	-60	8.5	128	3.5	450

3.3.1 Fixed Tuning Control Switches

As previously mentioned, the control switches used to turn the tuning transistors off was ommited in the design. This effect was illustrated in Figure 3.29. After testing in the lab and discovering the error, the switches were added and the design was retested in Cadence simulations. Figure 3.35 shows the magnitude response of the FIR filter when the missing switches are added. Bandwidth selections of 3, 10, and 25 MHz are shown. Also illustrated in the figure in the blue waveforms is the magnitude response when these switches are missing. As can be seen, much better performance is achieved when the tuning transistor gates are no longer floating.

3.4 Conclusions

This chapter introduces a programmable linear phase 128-tap FIR bandpass filter in a 0.18 μm Jazz SOI process. Although initially designed to operate at 40 MHz IF, due to the accidental ommision of the pull-down transistor in the tuning transistors of the tunable transconductors, the filter has a 20 MHz IF and is tunable in bandwidth from 1.5 to 15 MHz. Due to the nature of linear phase FIR filters, minimal group delay variations are observed in the filter's passband which is optimal for pulsed-Doppler radar systems since it allows the pulse's envelope to not be skewed. The filter has a mean IIP3 of 9.8 dBm (worst case of 8.5 dBm). The total integrated noise is a worst case of -49 dBm. The FIR filter architecture employs the cascade of four 32-tap sections coupled by four active multiplexer sections leading to an FIR filter of 128 taps. The filter is highly programmable in bandwidth thanks to the use of bias constant OTAs with widely adjustable transconductance. The OTA current is coherently integrated on a set of capacitors that are sequentially read through the active multiplexers employing a phase synthesizer that generates 34 non-overlapping clock phases. The architecture is suitable for high frequency operation since it is

based on current mode techniques.

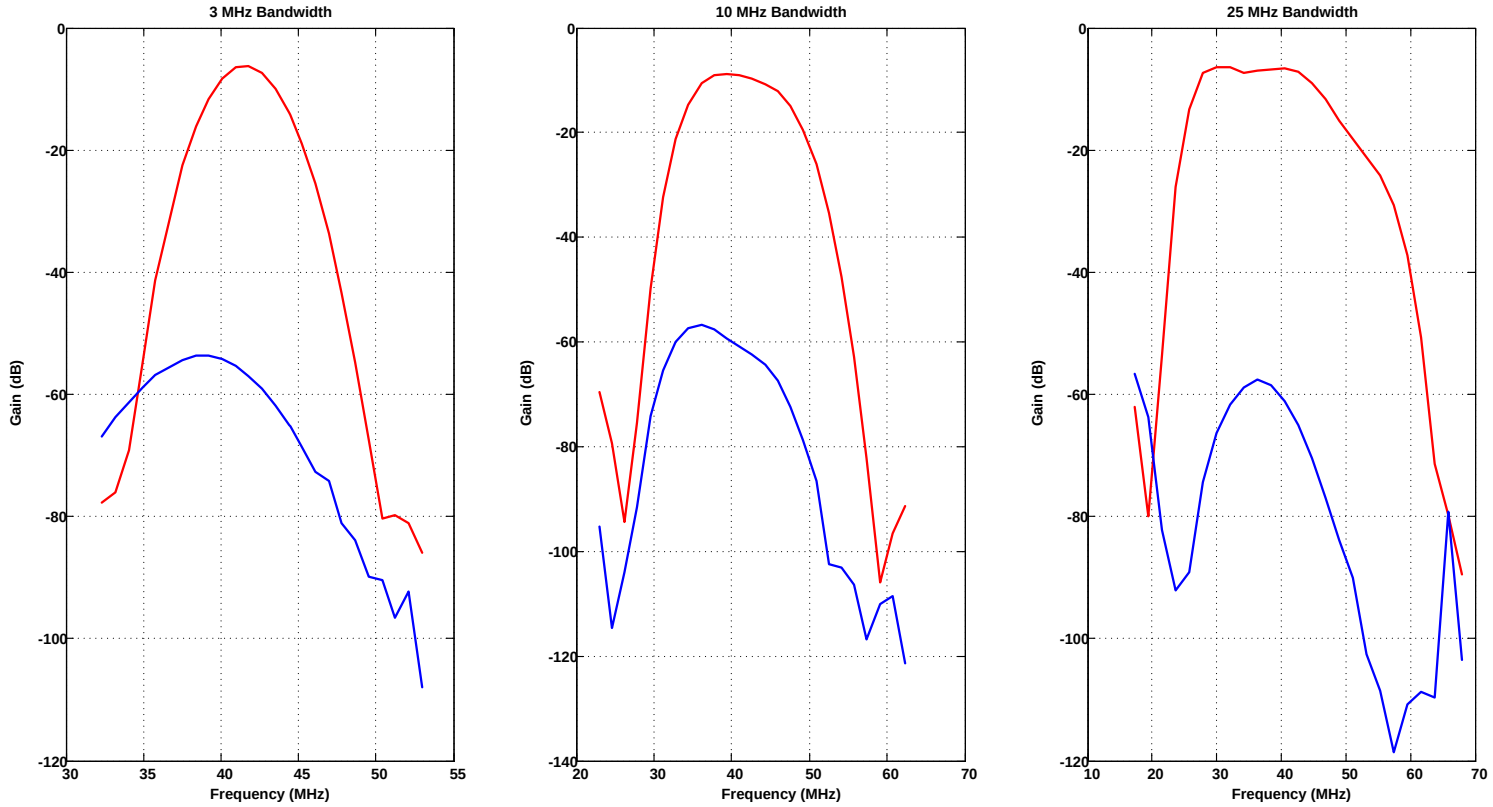


Figure 3.35: Magnitude response when the tuning control switches are fixed. 3 MHz, 10 MHz, and 25 MHz bandwidths are shown. The red waveforms show the corrected frequency response while the blue ones show what was actually fabricated and tested.

4. A BLOCKER-TOLERANT, HIGH-SENSITIVITY ΔΣ CORRELATION DIGITIZER FOR RADAR AND COHERENT RECEIVER APPLICATIONS

Delta-Sigma ($\Delta\Sigma$) modulators were first proposed in the 1960s as a method to reduce quantization noise in analog-to-digital converters (ADCs) by the use of a feedback network [53]. Since that time, $\Delta\Sigma$ modulators have become popular solutions in a variety of digitization solutions including ADCs for high resolution audio applications [54–56], biomedical systems [57–59], and cellular networks [60,61]. Bandpass $\Delta\Sigma$ modulators have recently become a popular method for direct RF digitization in many systems as they offer potential solutions for software defined radio [62–64]. $\Delta\Sigma$ based solutions have also been used in radar systems for few applications such as beamforming [65], but the full use of their benefits in radar systems has not yet been exploited.

In a Doppler radar system, a known reference signal is radiated from the antenna with the goal of determining the range and velocity of a target [3,52,66]. This transmitted signal may be a pure frequency tone, a frequency chirp, or it may have some modulation scheme encoded such as binary phase shift keying (BPSK). The received echo at the antenna will be a time-delayed version of the transmitted signal with some additional Doppler frequency shift dependent on the target's velocity. Unlike standard communication systems where the receiver must attempt to determine the transmitted information sequence, due to the modulation sequence being known *a priori* in radars, special techniques can be used to aid in the recovery of the received waveform to determine the target's range and velocity.

In very wide bandwidth linear frequency modulated (LFM) radars, the chirp waveform is sometimes demodulated with a process known as stretch processing in

order to reduce the signal bandwidth to ease processing of the signal [1]. Extending this approach to discrete-time analog processing, this paper presents a $\Delta\Sigma$ modulator based ADC used in conjunction with the known pseudorandom BPSK sequence in order to simultaneously demodulate and digitize the signal. The demodulation operation reduces the signal bandwidth allowing further filtering in the digital domain to improve SNR. Any interferers appearing at the input – even within the signal bandwidth – that are uncorrelated with the pseudorandom BPSK sequence will have their spectrums suppressed. This property produces a digitizer which is more tolerant to in-band blockers that often appear with much greater power than the desired echo signal.

4.1 Subsampling Coherent Digitizers

Figure 4.1 shows an example of a pulsed-Doppler radar transceiver. This system measures the range and velocity of a target by detecting the transit time and Doppler shift of a reflected RF modulated pulse [3, 52]. The transmitter consists of a pair of signal sources – a reference oscillator operating at f_{IF} and a voltage controlled oscillator (VCO) operating at the RF frequency f_{VCO}. The reference frequency is upconverted to $f_{VCO} - f_{IF}$, pulse modulated at a pulse repetition frequency (PRF) f_{PRF}, and modulated with a binary pseudorandom phase code. The resulting RF pulse is radiated from the antenna, to a target, and then reflected back to the antenna with some delay proportionate to the distance between antenna and target. The return signal also undergoes a Doppler shift in frequency f_D dependent on the velocity of the target. The received signal at $f_{VCO} - f_{IF} - f_D$ is amplified, bandpass filtered, down-converted to $f_{IF} + f_D$, and subsampled by an ADC at a rate greater than or equal to one sample per pseudorandom phase bit. The sampled signal is then processed by a digital signal processor (DSP) to recover the range and velocity

information.

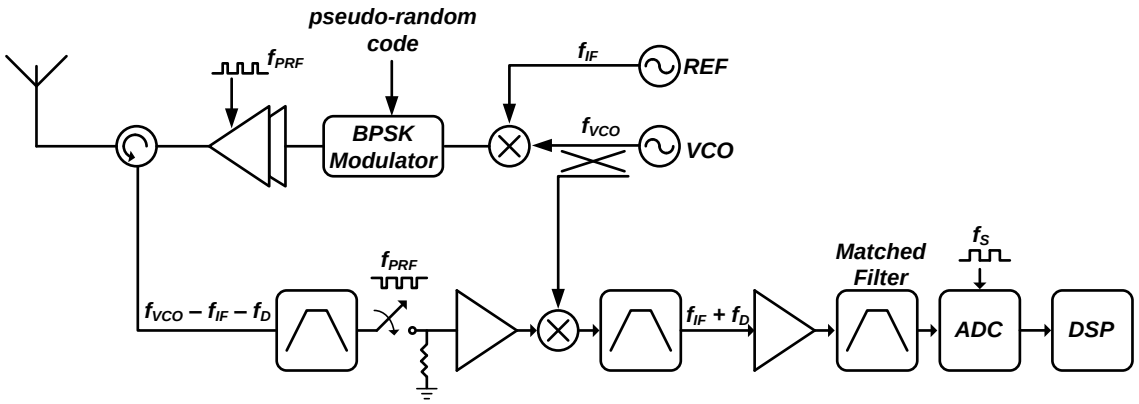


Figure 4.1: Block diagram of a pulsed-Doppler radar system with monobit subsampling.

In some radar systems, the input signal-to-noise ratio (SNR_{in}) is very low, perhaps as low as -50 dB. In these negative SNR_{in} scenarios, the power of in-band thermal noise and in-band blockers is much greater than the quantization noise of even a single-bit quantizer. Therefore, increasing the resolution of the quantizer will have no major improvement on the output signal-to-noise ratio (SNR_{out}). Due to this, it has been desirable to quantize with monobit subsamplers as illustrated in Figure 4.2a [3]. Receiver sensitivity is improved in the digital domain by integrating a series of pulses in order reduce the noise power by averaging. Integrating N pulses can improve the sensitivity by up to $10\log(N)$ dB which allows the detection of large negative SNRs at the receiver input with low sensitivity to the effects of phase noise [3, 67].

In the monobit subsampler of Figure 4.2a, DC offset can limit the sensitivity of the receiver. In [52], a single-bit quantizer with delta modulation was introduced

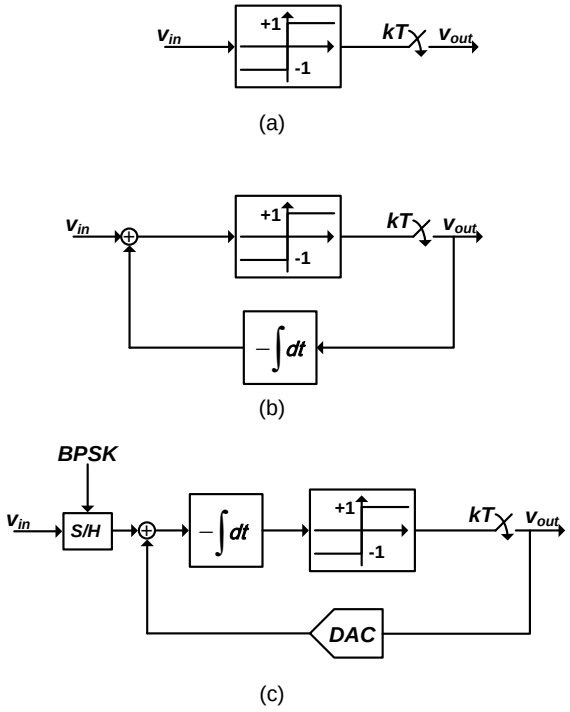


Figure 4.2: Digitization methods including (a) monobit subsampling, (b) delta modulation, and (c) the proposed $\Delta\Sigma$ correlation digitizer.

which improves the sensitivity by subtracting the time-average value of the output from the input; thus, any degradation due to DC offset is suppressed.

In both Figure 4.2a and Figure 4.2b, due to the pseudorandom BPSK modulation, the signal power that is recovered at baseband is spread over some bandwidth that is more than an order of magnitude larger than the frequency range of possible Doppler frequency offset. The received, digitized signal is then processed in the digital domain with operations such as 1) averaging to minimize thermal noise and 2) deconvolution of the BPSK sequence to obtain the Doppler frequency tone. Since in-band blockers can be stronger than the Doppler signal by even 40 dB or more, it is not trivial to recover the desired information.

In the following section, a new technique is presented to digitize the output of

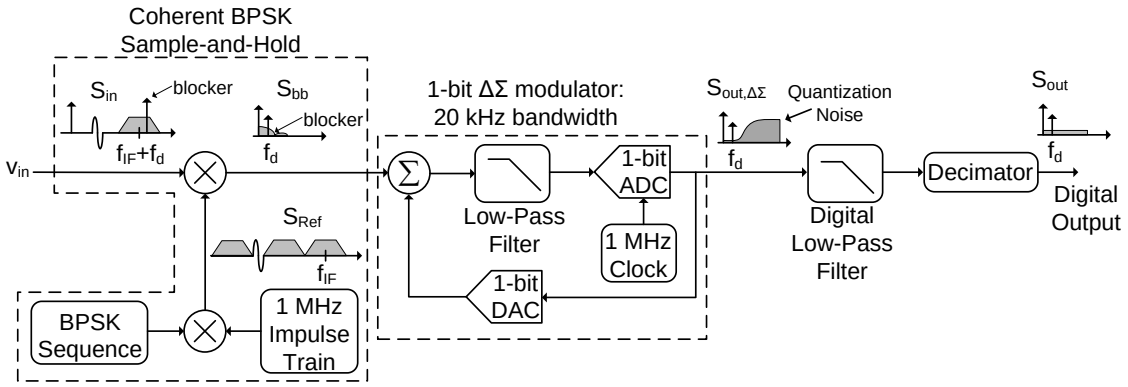


Figure 4.3: Block diagram of proposed receiver.

the matched filter which is briefly illustrated in Figure 4.2c. The BPSK information is removed during the subsampling process in order to reduce the bandwidth of the signal being quantized to a single frequency tone located at the Doppler frequency. At the same time, the remaining noise and blockers after the matched filter are convolved with the BPSK frequency thus spreading its energy over broader bandwidth. This allows out-of-band noise to effectively be filtered by the narrow-band ADC in order to improve system SNR_{out}.

4.2 Proposed Coherent Receiver Design

The proposed $\Delta\Sigma$ correlation digitizer design is illustrated in Figure 4.3. The input signal is assumed to have a pseudo-random ± 1 BPSK modulation. Because the precise BPSK sequence is known to the system *a priori* at the time of transmission, it can be directly removed in the ADC's sample-and-hold process. Consider the received signal which contains the desired BPSK modulated pulse along with some

blocker at frequency f_b. This waveform is given by the expression

$$\begin{aligned} V_{in}(t) = BPSK(t - t_D) \times A_d \sin\left(2\pi\left(f_{IF} + f_D\right)(t - t_D)\right) \\ + A_b \sin(2\pi f_{IF,b} t) \end{aligned} \tag{4.1}$$

where *BPSK(t)* is the ± 1 modulation as a function of time, t_D is how much time delay has occured due to the propagation of the radar pulse, A_d and A_b are the amplitude of the desired signal and blocker, respectively, f_D is the Doppler frequency impressed upon the received signal by the target, and $f_{IF,b}$ is the downconverted frequency of the blocker. By multiplying the received signal by a properly time-delayed version of the BPSK sequence, the BPSK randomization is removed from the signal of interest and impressed upon the undesired blocker tone giving the demodulated input signal

$$\begin{aligned} V_{in,demod}(t) = A_d \sin\left(2\pi\left(f_{IF} + f_D\right)(t - t_D)\right) \\ + BPSK(t - t_D) \times A_b \sin(2\pi f_{IF,b} t) \end{aligned} \tag{4.2}$$

since $BPSK^2(t - t_D) = 1$. This is straightforward to do in the sample-and-hold process because only a muliplication by ± 1 is required. When BPSK $= +1$, the signal is passed as is; when BPSK $= -1$, an inversion is applied. In (4.2), the blocker tone located at $f_{IF,b}$ is BPSK modulated which will spread its energy across a wide spectrum. A non-return-to-zero BPSK pulse with ± 1V amplitude has the power spectral density (PSD)

$$S_{BPSK}(f) = T\left(\frac{\sin \pi f T}{\pi f T}\right)^2 \tag{4.3}$$

where T is the symbol period. A blocker at frequency f_b with amplitude A_b will thus be BPSK modulated by the PN23 sequence resulting in the spectrum

$$S_b(f) = \frac{A_b^2 T}{2} \left(\frac{\sin \pi (f - f_{IF,b}) T}{\pi (f - f_{IF,b}) T} \right)^2 \tag{4.4}$$

which has a peak power T times less than the original blocker tone. For a 1 MHz clock rate, for example, this is a $10 \log(1 \times 10^{-6}) = -60$ dB suppression of the blocker tone peak value in the output spectrum; the power of the blocker tone is spread over a frequency range of 2-3 times the clock frequency. Furthermore, because the desired Doppler tone is, for most applications, orders of magnitude lower than the BPSK modulation bandwidth, the majority of the broadband blocker PSD can be removed.

After the input signal in Figure 4.3 is demodulated in the sample-and-hold process, it is then digitized with a $\Delta\Sigma$ modulator sampled at f_{PRF}. In this dissertation, it is assumed that f_D is limited to the range of 0 – 20 kHz. The resulting digitized signal at the output of the $\Delta\Sigma$ modulator can then have all of the out-of-band noise low-pass filtered in the digital domain (e.g., in a decimation process), thus achieving better SNR at the digitizer output than was originally applied to the input of the digitizer.

The implementation of the sample-and-hold circuit and $\Delta\Sigma$ modulator of Figure 4.3 is illustrated in Figure 4.4, ignoring R_2 and C_2 for now. The circuit is controlled by two main non-overlapping clock phases ϕ_1 and ϕ_2, which can easily be generated [68].

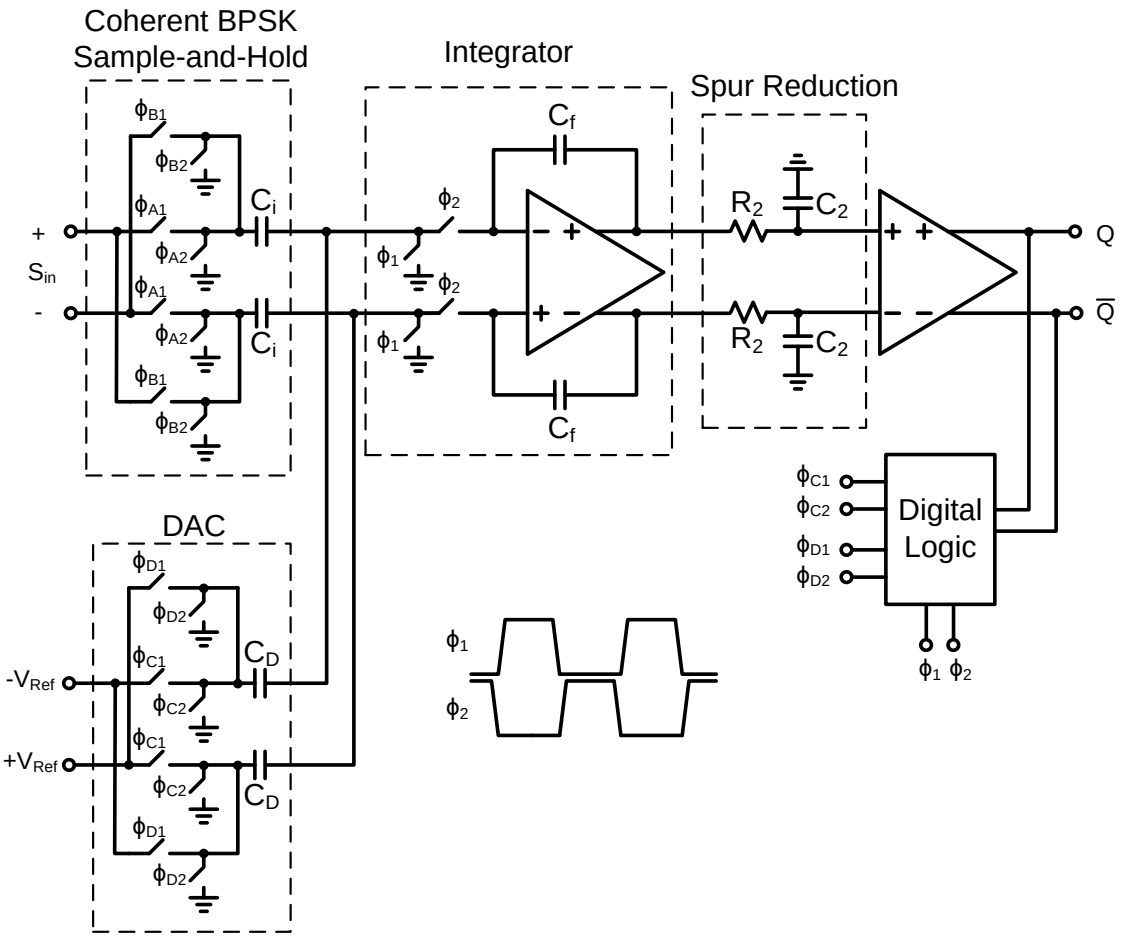


Figure 4.4: Implementation of proposed coherent digitizer.

The BPSK demodulation is implemented by the switches at the input which are controlled by clock phases ϕ_{A1}, ϕ_{A2}, ϕ_{B1}, and ϕ_{B2}. These are expressed with simple logic functions

$$\begin{aligned} \phi_{A1} &= P \times \phi_1 \\ \phi_{A2} &= P \times \phi_2 \\ \phi_{B1} &= \overline{P} \times \phi_1 \\ \phi_{B2} &= \overline{P} \times \phi_2 \end{aligned} \tag{4.5}$$

where P represents the properly time delayed BPSK sequence that was applied to the transmitted waveform, $BPSK(t - t_D)$. If P is 1, then $\phi_{A1} = \phi_1$, $\phi_{A2} = \phi_2$, and $\phi_{B1} = \phi_{B2} = 0$ and the input signal passes as is. If P is 0, then $\phi_{B1} = \phi_1$, $\phi_{B2} = \phi_2$, and $\phi_{A1} = \phi_{A2} = 0$ and the input signal is inverted.

Following these sample-and-hold switches is the discrete-time first-order $\Delta\Sigma$ modulator. The architecture employs a single-bit quantizer and single-bit switched-capacitor DAC. The switched-capacitor DAC consists of an array of switches that connect the feedback capacitors to $+V_{Ref}$ or $-V_{Ref}$ during ϕ_2 according to whether the comparator's output Q is 1 or 0. The logic for the implementation of the clocks in the DAC is

$$\begin{aligned} \phi_{C1} &= Q \times \phi_1 \\ \phi_{C2} &= Q \times \phi_2 \\ \phi_{D1} &= \overline{Q} \times \phi_1 \\ \phi_{D2} &= \overline{Q} \times \phi_2. \end{aligned} \tag{4.6}$$

The signal transfer function (STF) of this first order $\Delta\Sigma$ modulator is

$$STF(z) = \frac{\left(\frac{C_i}{C_f}\right)\left(\frac{z^{-1}}{1-z^{-1}}\right)}{1 + \left(\frac{C_D}{C_f}\right)\left(\frac{z^{-1}}{1-z^{-1}}\right)} = \frac{\left(\frac{C_i}{C_f}\right) z^{-1}}{1 + \left(\frac{C_D}{C_f} - 1\right) z^{-1}} \tag{4.7}$$

while the noise transfer function (NTF) is

$$NTF(z) = \frac{1}{1 + \left(\frac{C_D}{C_f}\right)\left(\frac{z^{-1}}{1-z^{-1}}\right)} = \frac{1 - z^{-1}}{1 + \left(\frac{C_D}{C_f} - 1\right) z^{-1}} \tag{4.8}$$

Assuming $C_i = C_d = C_f$, the signal transfer function simplifies to

$$STF(z) = z^{-1} \tag{4.9}$$

while the noise transfer function is reduced to

$$NTF(z) = 1 - z^{-1}. \tag{4.10}$$

Notice from (4.9) the loop's integrator does not filter the input signal. In a typical application employing a $\Delta\Sigma$ modulator such as this, the input must be band-limited to less than $f_s/2$ to avoid aliasing issues. This is not necessarily the case here due to the BPSK modulation/demodulation that is applied at the input which will suppress out-of-band signals, essentially making them appear as noise; however, it is beneficial to filter out-of-band signals beforehand to keep the noise floor low.

Assuming that the quantization noise is random with a noise power density given by $Q^2(z)$, then the first order approximation of the in-band signal-to-quantization noise ratio (SQNR) can be obtained as

$$\begin{aligned} SQNR &= \frac{P_{in}\left|z^{-1}\right|^2}{\left|\int_0^{f_{BW}}\left(Q(z)NTF(z)\right)^2 df\right|} \\ &\cong \left(\frac{P_{in}}{\left|Q(z)\right|^2 f_{BW}}\right)\left|\frac{f_{BW}}{\int_0^{f_{BW}}\left(2\sin\left(\frac{\omega T}{2}\right)\right)^2 df}\right| \\ &\cong \left(SQNR_{quantizer}\right)\left|\frac{f_{BW}}{\int_0^{f_{BW}}\left(2\sin\left(\frac{\omega T}{2}\right)\right)^2 df}\right| \end{aligned} \tag{4.11}$$

where P_{in} is input power of the desired signal, $SQNR_{quantizer}$ is the SQNR of the standalone single bit quantizer, f_{BW} is the maximum expected Doppler offset frequency, considered to be 20 kHz in this design, and T is the period of the sample

clock, or $1/f_S$. Equation (4.11) can be approximated as

$$\begin{aligned} SQNR &\cong (SQNR_{quantizer}) \left(\frac{3}{\pi^2} \times \left(\frac{f_S}{2f_{BW}} \right)^3 \right) \\ &\cong (SQNR_{quantizer}) \left(\frac{3}{\pi^2} \times OSR^3 \right) \end{aligned} \tag{4.12}$$

In a first order approximation, the SQNR of the $\Delta\Sigma$ modulator improves $-5.2 + 30\log(OSR)$ dB with respect to the quantizer's SQNR. Employing the classic equation for SQNR of the standalone quantizer, given by $6.02N + 1.76$ where N is the number of bits in the quantizer, (4.12) reduces to

$$\begin{aligned} SQNR_{dB} &= 6.02 + 1.76 - 5.2 + 30\log(OSR) \\ &= 2.58 + 30\log(OSR) \end{aligned} \tag{4.13}$$

The circuit of Figure 4.4 is simulated with a BPSK modulated input located at the 40 MHz IF with a 4 kHz Doppler, and the resulting output spectrum is shown in Figure 4.5. As is typical in first-order $\Delta\Sigma$ modulators, there are several frequency spurs which hinder the performance [69]. In order to reduce the spurious tones, an additional simple first-order lowpass filter is added between the amplifier and comparator consisting of elements R_2 and C_2 as shown in Figure 4.4. This filter reduced the spurious tones by approximately 10 dB as will be seen in the measurement results.

Equation (4.13) is what the output SNR would be for an input with large SNR. For noisy inputs, however, the output SNR will be less than what (4.13) predicts. Typically, the input signal bandwidth will be greater than the sample rate of the quantizer f_s resulting in out-of-band noise folding back into the baseband spectrum raising the noise floor. This effect is illustrated by Figure 4.6a and Figure 4.6b.

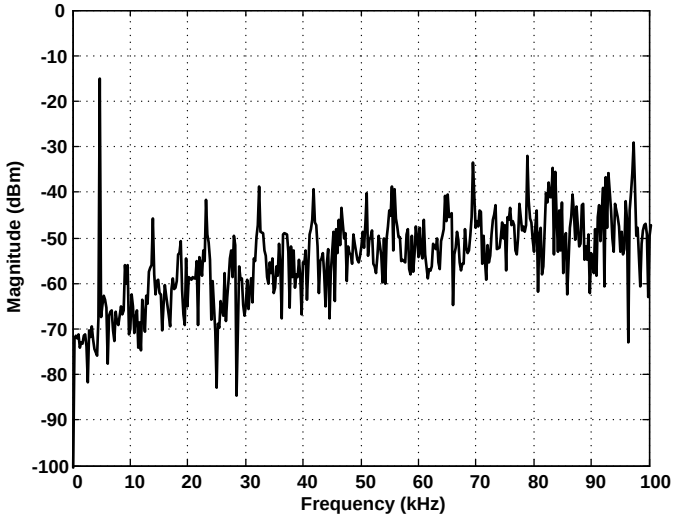


Figure 4.5: Simulated FFT of the digitizer output with a first order $\Delta\Sigma$ modulator with a 40.004 MHz BPSK modulated input.

When the noise above the maximum expected Doppler frequency is filtered by the digital lowpass filter following the $\Delta\Sigma$ modulator, the SNR will increase as shown in Figure 4.6c.

Assuming the input noise is limited to a noise equivalent bandwidth, f_{NEB}, the in-band (0–20 kHz) SNR will be limited to

$$\begin{aligned} SNR_{out} = SNR_{in} + 10\log(OSR) \\ - 10\log\left(\frac{f_{NEB}}{f_s}\right) \end{aligned} \tag{4.14}$$

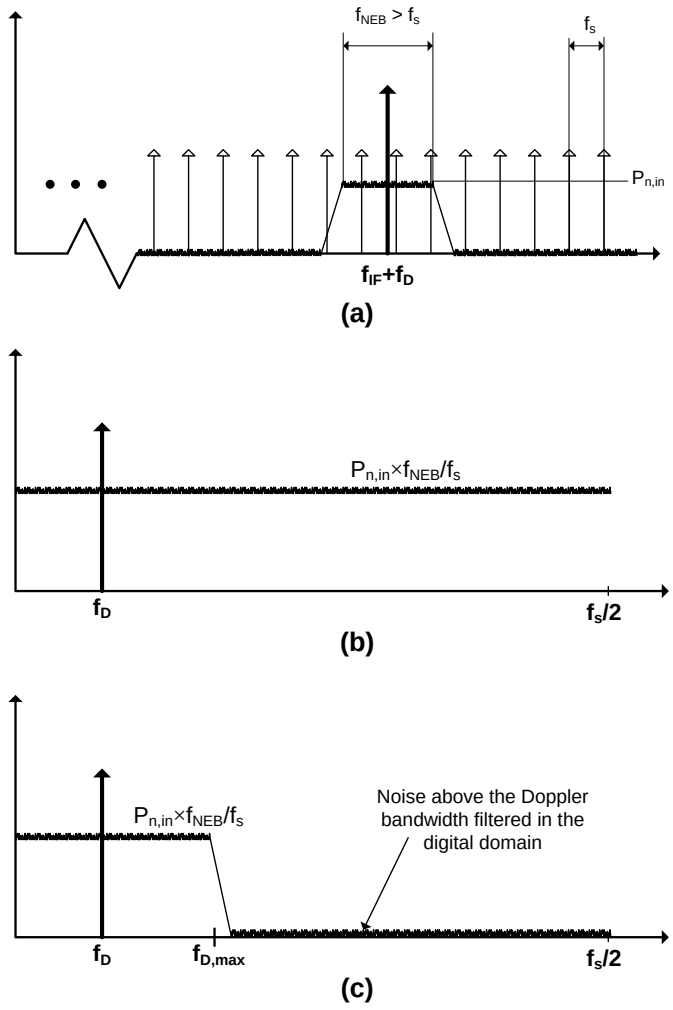


Figure 4.6: Subsampling process in the frequency domain. (a) Subsampling of the filtered IF signal, (b) effect of noise aliasing at baseband, and (c) out-of-band noise being filtered by the DSP.

Assuming that the Doppler bandwidth is limited to 20 kHz, the OSR is 25 when sampled at $f_s = 1$ MHz. For input signal bandwidths less than 25 MHz, the output SNR will be greater than the input SNR after lowpass filtering of the digitized samples. As an example, if the matched filter bandwidth is 10 MHz, the output noise will be 3.9 dB better than the input SNR until the thermal noise becomes lower than the quantization noise. At this point the SNR will be limited by (4.13) which is 44.5 dB when the OSR is 25. This example is illustrated in Figure 4.7.

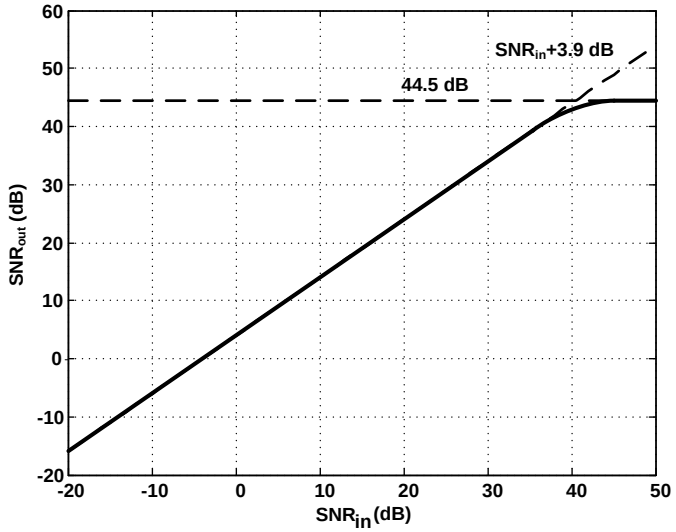


Figure 4.7: Output SNR vs Input SNR for case of 20 kHz Doppler bandwidth, sampled at 1 MHz, with a matched filter bandwidth of 10 MHz.

4.3 Circuit Implementation

The architecture of Figure 4.4 was designed in a TowerJazz 0.18 μm CMOS SOI process [18]; capacitors C_i, C_D, and C_f are each 1 pF. The RC network of R_2 and C_2 added for spur reduction consists of 50 kΩ resistors and 40 pF capacitors. The BPSK modulation used is a pseudorandom PN23 sequence. The reference voltage

for the DAC is 200 mV resulting in a 400 mV differential for the full scale amplitude. The $\Delta\Sigma$ modulator is sampled at 1 MHz resulting in an OSR of 25 for a 20 kHz signal bandwidth. The expected peak SQNR from (4.13) is 44.5 dB.

The amplifier used in the integrator of the $\Delta\Sigma$ modulator is a folded cascode amplifier which is shown in Figure 4.8 which uses the same bias circuitry that was illustrated in Figure 3.10. Transistor dimensions for the amplifier are listed in Table 4.1. The amplifier's performance was simulated in Cadence both with and without the additional filtering provided by R_2 and C_2. Figure 4.9a shows the loop gain of the OTA without R_2 and C_2. The low frequency gain is approximately 46 dB with a phase margin of 86°. The unity gain frequency is 69 MHz. When R_2 and C_2 are added, the loop gain changes to the plot illustrated in Figure 4.9b. The low frequency gain is approximately the same. The unity grain frequency decreases slightly to 64 MHz and raises the phase margin to 91°.

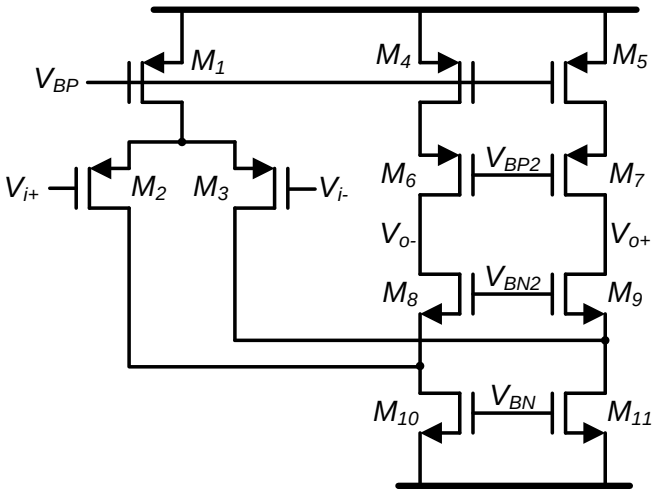


Figure 4.8: Schematic of amplifier used in $\Delta\Sigma$ integrator.

The input referred noise is pictured in Figure 4.10. At high frequency beyond

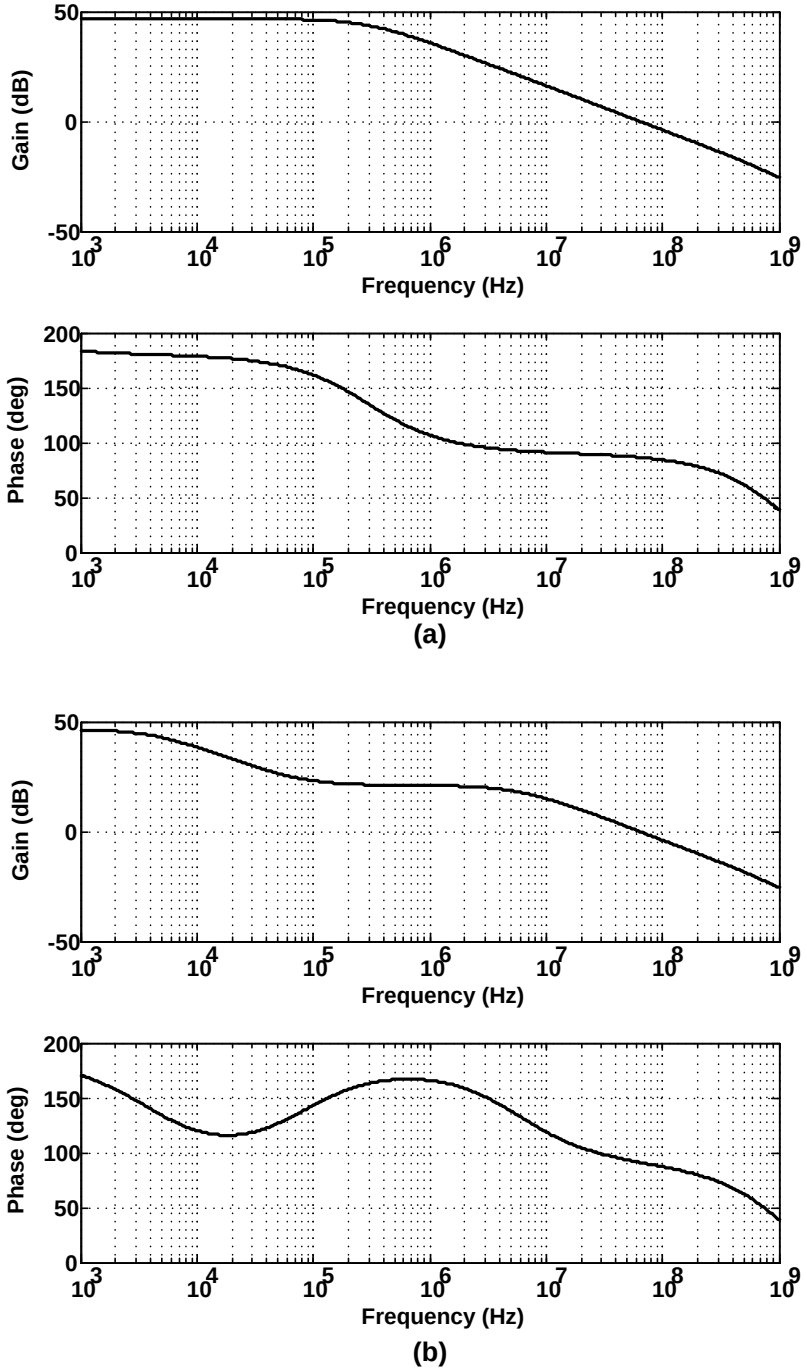


Figure 4.9: Loop gain response of the OTA (a) without the additional filtering provided by R_2 and C_2 and (b) including R_2 and C_2.

Table 4.1: Transistor dimensions for OTA of Figure 4.8.

Transistor	Size (μm)
M_1	$\frac{40}{0.4}$
M_2, M_3, M_4, M_5, M_6, M_7	$\frac{20}{0.4}$
M_8, M_9	$\frac{5}{0.4}$
M_{10}, M_{11}	$\frac{10}{0.4}$

the $1/f$ noise corner, the noise density is 18 nV/Hz$^{1/2}$. The integrated noise power from 1 kHz to 1 GHz is approximately -51 dBm. This value is low enough for the system as is; however, much of this noise will fall out-of-band improving the noise performance of the system.

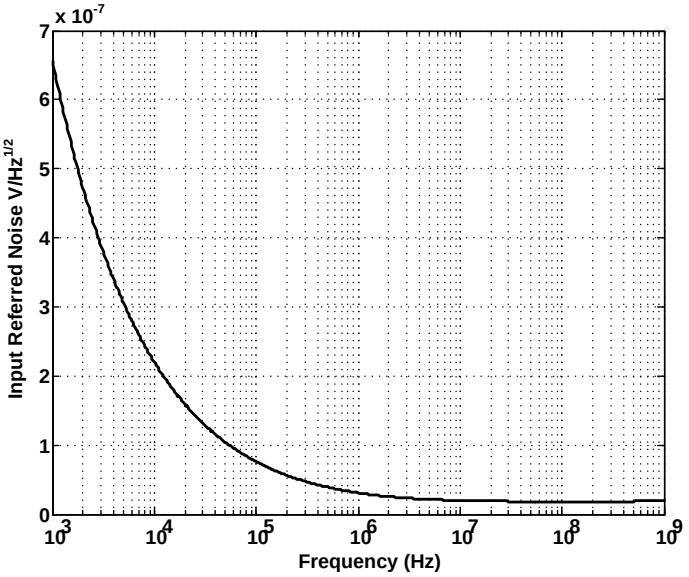


Figure 4.10: Input referred noise spectral density of the OTA.

Figure 4.11 shows the comparator used for the sampling operation which is a

dynamic comparator. Transistor dimensions for the comparator are listed in Table 4.2. When the sample clock signal goes high, the comparator makes a decision, pulling one output up to V_{DD} and the other down to ground. This causes the following SR-latch to set the output to either 0 or 1. When the clock signal goes low, both of the comparator outputs are pulled to V_{DD} causing the SR-latch to hold its value until the next sample phase.

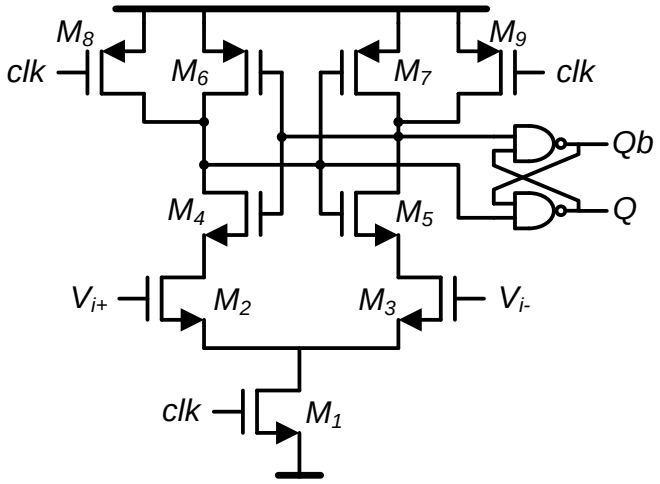


Figure 4.11: Schematic of comparator used with SR latch used to hold the output bit when the comparator is being reset.

Table 4.2: Transistor dimensions for comparator of Figure 4.11.

Transistor	Size (μm)
M_1, M_2, M_3	$\frac{5}{0.18}$
M_4, M_5	$\frac{2}{0.18}$
M_6, M_7	$\frac{6}{0.18}$
M_8, M_9	$\frac{2}{0.18}$

4.4 Measurement Results

The proposed coherent monobit subsampling receiver was designed and fabricated in TowerJazz 0.18 μm CMOS SOI process. The chip microphotograph is shown in Figure 4.12. The active area for the chip is 225 μm by 550 μm for a total active area of 0.124 mm^2. The total power consumption for the digitizer is 1.12 mW which includes the power consumption of the $\Delta\Sigma$ modulator, non-overlapping clock generator, and all digital logic.

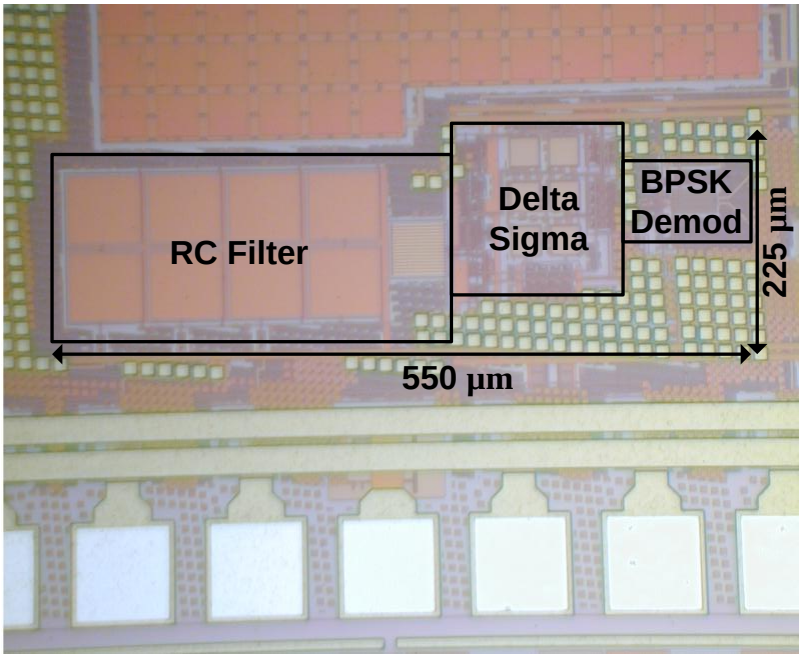


Figure 4.12: Microphotograph of fabricated chip.

The measurement setup for the characterization of the coherent digitizer is shown in Figure 4.13. A signal generator was used to supply an input at 40.00409 MHz which is BPSK modulated with a PN23 pseudorandom sequence. The 4.09 kHz shift in frequency from the 40 MHz IF was chosen to emulate a Doppler shift. This tone is

added with a power combiner to either another signal generator output representing a blocker tone or a noise source, depending on the current measurement. The combined signal is then converted to a differential signal on the PCB and applied to the coherent digitizer. The BPSK sequence is also provided to the device under test (DUT) along with a 1 MHz reference clock used in the generation of the non-overlapping clock phases ϕ_1 and ϕ_2. The output bit stream is buffered with an inverter chain and captured with a digital signal analyzer. The output data was then analyzed on a computer in MATLAB to quantify all measurement results.

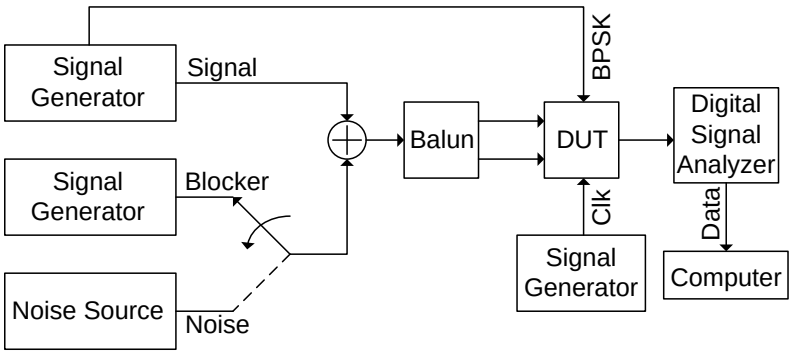


Figure 4.13: Measurement setup used to characterize the operation of the digitizer.

The downconverted output of the digitizer is shown in Figure 4.14 given a -15 dBm (with respect to 50 Ω), 40.00409 MHz BPSK modulated input with the ΔΣ clocked at 1 MHz. Figure 4.14a shows the time-domain output with the characteristic pulse width modulated output that is typical in single-bit ΔΣ modulators. The output spectrum is shown in Figure 4.14b which illustrates the noise shaping behavior of the ΔΣ ADC.

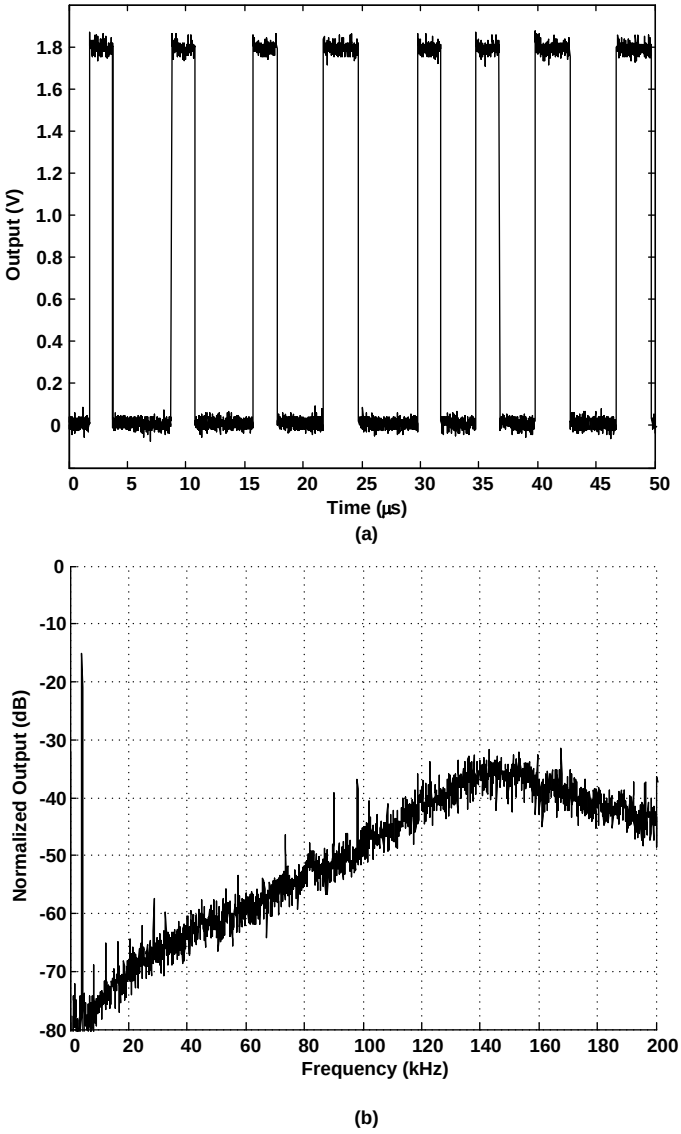


Figure 4.14: Downconverted output of the digitizer for -15 dBm input. (a) Time-domain waveform showing the pulse width modulated output that is typical of $\Delta\Sigma$ modulators, and (b) the normalized output spectrum showing the noise shaping behavior.

To measure the linearity of the $\Delta\Sigma$ modulator based digitizer, two tones were generated at 40.004 MHz and 40.005 MHz. The BPSK modulation from the source was disabled for this measurement due to functionality limitations in the signal generator. The input power was swept, and the output spectrum was computed in MATLAB. Figure 4.15 shows the results for the linearity measurements. The IIP3 can be extrapolated to be 7.5 dBm. Any nonlinearities that are introduced at the input due to the source or input switches will appear at integer multiples of the $f_{IF} + f_D$ which alias back to baseband due to the subsampling. These terms are in addition to the nonlinearities introduced by the $\Delta\Sigma$ modulator.

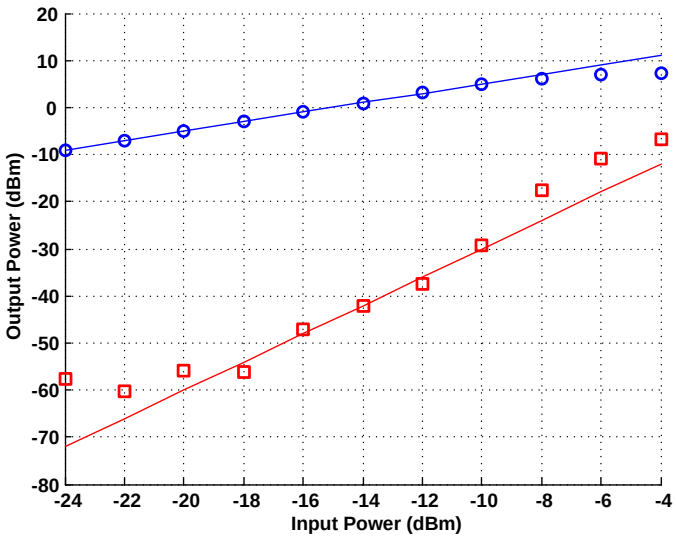


Figure 4.15: Linearity measurement for the digitizer. Fundamental and IM3 components are plotted.

In order to measure the in-band blocker tolerance of the receiver, a non-modulated blocker tone at 40.006 MHz was added to the BPSK modulated input signal at 40.00409 MHz with a power combiner. The signal tone used has an input power of

-45 dBm while the blocker power is swept from -45 dBm to -5 dBm. As an example, Figure 4.16a shows the input spectrum when the blocker tone is -15 dBm, or 30 dB greater than desired signal. The power of the input signal is *sinc* distributed since the Doppler tone is BPSK modulated by the pseudorandom sequence. Figure 4.16b shows the spectrum of the output of the digitizer. The Doppler tone at 4.09 kHz is the only visible tone. The blocker has been randomized in front of the $\Delta\Sigma$ modulator and now appears as in-band noise distributed over 1 MHz bandwidth approximately 50 dB lower than the initial power of the blocker tone. This is close to what is predicted by (4.4). Due to the additional sidelobes of the *sinc* function that alias in-band, the noise floor is slightly higher than (4.4) suggests.

Figure 4.17 shows how increasing the blocker power raises the noise floor at the output of the $\Delta\Sigma$ modulator. Figure 4.18 shows the SNR of the output signal assuming the out-of-band noise is removed by the DSP. The bandwidth for noise integration is assumed to be DC to 20 kHz. For small blocker powers, the noise level of the output spectrum is defined by the quantization noise of the digitizer. As the blocker power increases, the noise floor will rise decreasing the SNR. When the blocker power is -5 dBm, or 40 dBm greater than the signal, the signal tone will become buried in the noise floor and additional averaging will be required to recover the signal with enough resolution.

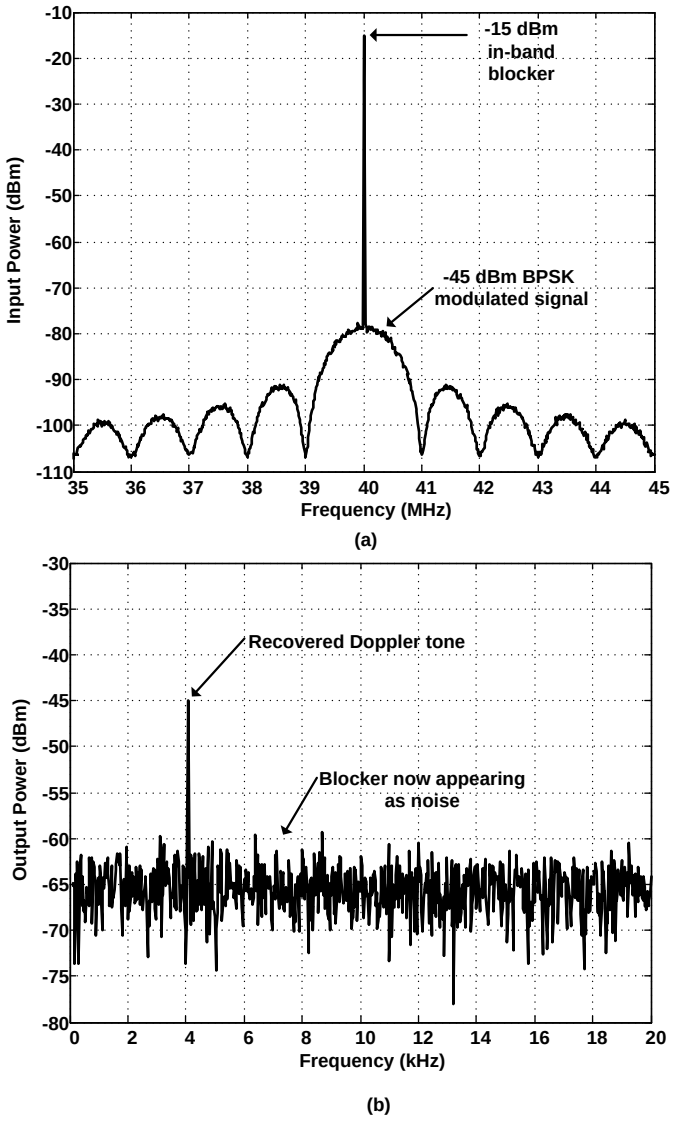


Figure 4.16: In-band blocker tolerance demonstration. (a) Input spectrum with -45 dBm signal BPSK modulated with a -15 dBm blocker tone near $f_{IF} + f_D$ and (b) the baseband output spectrum showing the recovered Doppler tone with the blocker suppressed and appearing as noise.

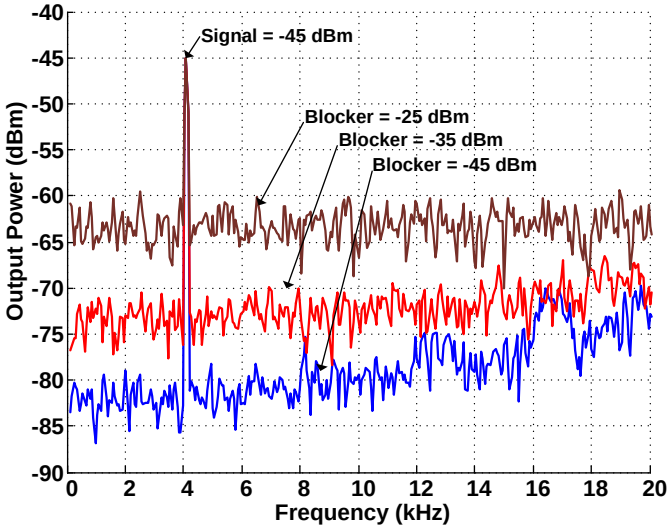


Figure 4.17: Noise floor increases with blocker power linearly.

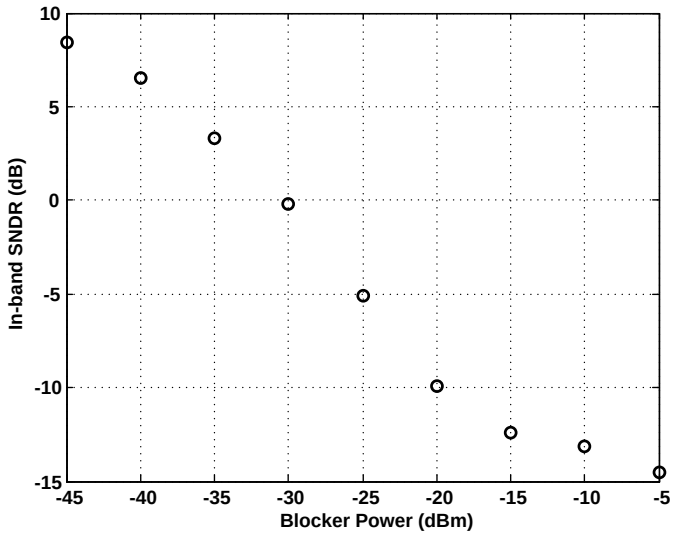


Figure 4.18: In-band SNR when sweeping blocker power. Input power is fixed at -45 dBm.

To measure the tolerance of the digitizer to noise, the input signal is added to a noise source through a power combiner. The noise source used is a NoiseCom NC1107A source which produces a white noise from 100 Hz to 100 MHz. This noise was filtered with a passive 30 MHz bandpass filter centered at approximately 40 MHz and adjusted to the desired level using in-line attenuators. Figure 4.19 shows the input spectrum of the signal after the bandpass filter when the input SNR to the $\Delta\Sigma$ modulator is -10 dB. Also shown in this figure is the signal spectrum with no noise added. As can be seen, the signal is buried below the noise floor. After digitization, the output spectrum that is obtained is shown in Figure 4.20. The Doppler tone is clearly visible. Due to the out-of-band noise folding back in-band due to the subsampling, the noise floor rises. Since the input bandwidth to sample rate ratio is greater than the OSR of the $\Delta\Sigma$ modulator, the SNR slightly decreases to -12 dB as can be expected from (4.14).

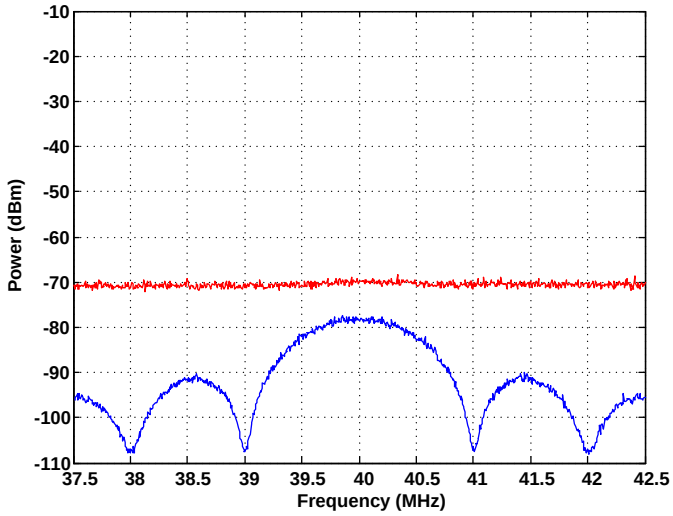


Figure 4.19: The red top waveform is the -10 dB SNR input spectrum. The blue bottom waveform shows the input spectrum without noise added.

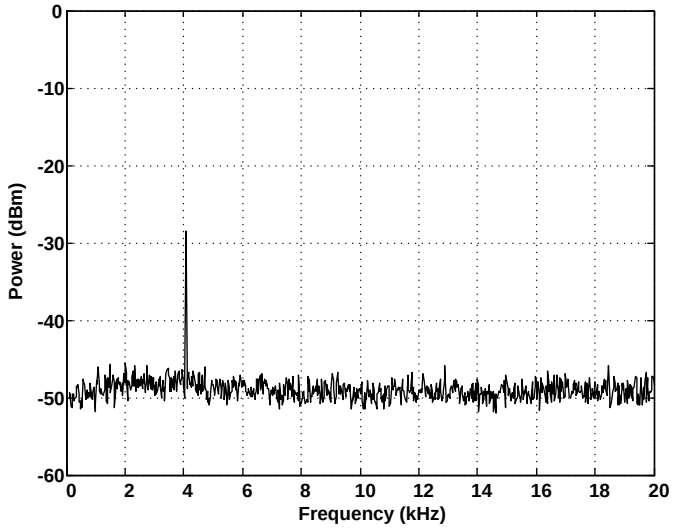


Figure 4.20: Digitized output spectrum when input SNR is -19 dB. SNR at the output is approximately -12 dB when noise is integrated up to 20 kHz.

To measure the SQNR or the $\Delta\Sigma$ modulator, the input power was swept with a BPSK modulated input at 40.00409 MHz; no blockers or additional noise were added. Figure 4.21 shows the SQNR plot measurement. The peak value of the SQNR is 43.6 dB which is approximately 7 bits. This corresponds well to what is predicted by (4.13). All of the measurement results described above are summarized in Table 4.3.

4.5 Conclusion

In this paper a technique to demodulate and digitize a received pulse for a pulsed Doppler radar system has been presented. By knowing the BPSK information sequence *a priori*, a time-delayed BPSK sequence range-matched to the target can be applied to the input to demodulate the received signal and suppress all in-band and out-of-band blockers before being processed by the digitizer.

After demodulation of the received pulse in the analog domain, a $\Delta\Sigma$ modulator

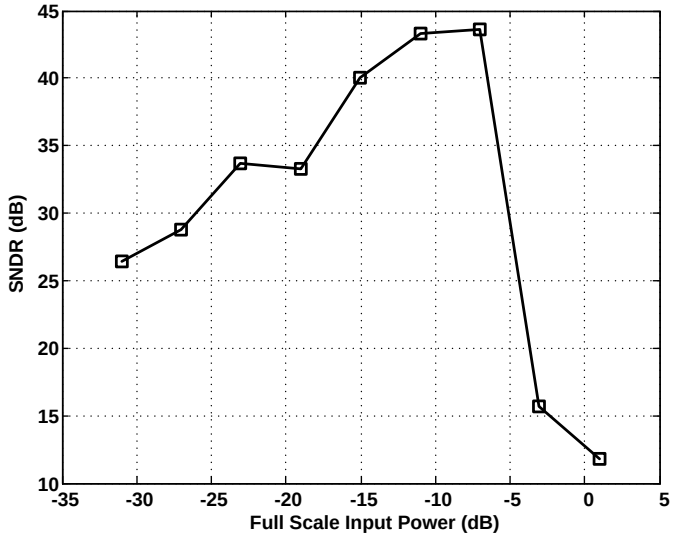


Figure 4.21: In-band SQNR when no blockers are present. Input power is relative to the full scale input voltage defined by $\pm V_{ref}$

Table 4.3: Summary of measurement results.

Measurement	Value
Technology	0.18 μm SOI
Chip area	0.124 mm^2
Power	1.12 mW
IIP3	7.5 dBm
Blocker Rejection	50 dB
Maximum SQNR	43.6 dB

subsamples and digitizes the received pulse to recover the Doppler tone. Since the bandwidth of the output signal is decreased from the input, total integrated noise can be reduced resulting in an improved SNR at the digitizer's output provided that the preceding matched filter's bandwidth is small enough.

The digitizer achieves 7.5 dBm IIP3 with a power consumption of 1.12 mW. Based on a simple switched-capacitor $\Delta\Sigma$ modulator, the proposed approach is a

simple method to improve the SNR of the received Doppler-shifted pulse while being resilient to blockers that are up to 40 dBm larger than the desired signal.

5. CONCLUSION

In the preceeding chapters, a matched filter has been presented for pulsed Doppler radars. A radar matched filter is one that provides the ideal response for a given pulse shape. It must have a small enough bandwidth in order to maximize the output SNR while being sufficiently large in bandwidth to pass the pulse without excessive spreading in time. The radar matched filter must also have a linear phase response as well to avoid any additional time-domain skewing.

An FIR filter has been presented which is widely tunable in bandwidth while having a flat group delay response due to its FIR nature. Centered at 40 MHz, the bandwidth is tunable from 3 to 30 MHz in order to be optimized for varying pulse widths. Bandwidth tuning is made possible with a unique tuning scheme allowing a large degree of selectivity in transconductance. The FIR filter is comprised of 128 taps which provides more than 50 dB attenuation just 10 MHz beyond the corner frequency. While using more power than past FIR filter approaches, this is the first bandpass filter presented which is widely tunable in bandwidth without changing the sample rate.

Because of the discrete-time nature of the FIR topology, an antialias filter should be used prior to the FIR filter to attenuate out-of-band frequencies which may fold back into the filter's passband. A novel G_m-C biquadratic filter has been presented which has shown to have excellent power efficiency. Based on differential difference amplifiers, the presented biquad topology reuses bias current between two differential pairs to reduce power consumption without hindering noise performance. A 6th order Butterworth filter was designed as a proof of concept which consumes just 1.34 mW per pole while having an IIP3 of 12 dB and 40 $nV/Hz^{1/2}$ input referred noise.

Finally, a coherent digitizer based on a $\Delta\Sigma$ modulator was presented which is able to recover the Doppler frequency tone embedded in the received pulse. By using the BPSK modulation information that the transmitted waveform is encoded with, the receiver is able to demodulate the received pulse prior to sampling. This operation reduces the received signal bandwidth from the low MHz range to just 20 kHz, the maximum expected Doppler frequency. This allows for a $\Delta\Sigma$ modulator to subsample the pulse providing just the unmodulated Doppler tone visible at baseband. Out-of-band thermal and quantization noise can then be filtered by the DSP to provide an improved SNR at the output without any additional averaging operations.

A secondary benefit of demodulating the signal prior to sampling is that all interferers that are uncorrelated with the pseudorandom BPSK sequence have their frequency spectrums suppressed making them appear as noise. Detection of Doppler tones in the presence of blockers 40 dB more powerful than the signal is easily manageable without any additional post-processing improvements. The digitizer achieves this while only consuming 1.12 mW from a 1.8 V supply. The peak SNDR is 43 dB.

The techniques presented in this dissertation are new methods to handle problems that arise in radar receivers which allow for potential monolithic solutions. These reduced complexity solutions can allow for less complex receivers at a more affordable cost without sacrificing performance.

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